Schematic Page List Hide

- X541UV_MB_PR_20160616-01
  - 001_Block Diagram
  - 002_System Setting
  - 003_CPU_DISPLAY
  - 004_CPU_DDR4
  - 005_CPU_LPC,SPI,SMB,CLINK
  - 006_CPU_POEWR
  - 007_***
  - 008_CPU_MISC,JTAG
  - 009_CPU_CFG,RSVD
  - 010_CPU_POWER_CAP
  - 011_NB_****
  - 012_NB_****
  - 013_DDR4_TERMINATION_A
  - 014_DDR4_ON-BOARD_A_L32
  - 015_DDR4_ON-BOARD_A_H32
  - 016_DDR4_****
  - 017_DDR4_SO-DIMM_1
  - 018.DDR4_CA VOLTAGE
  - 019_DDR4_****
  - 020_CPU_PCH_CSI2,EMMC
  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC

SYSTEM PAGE REF.

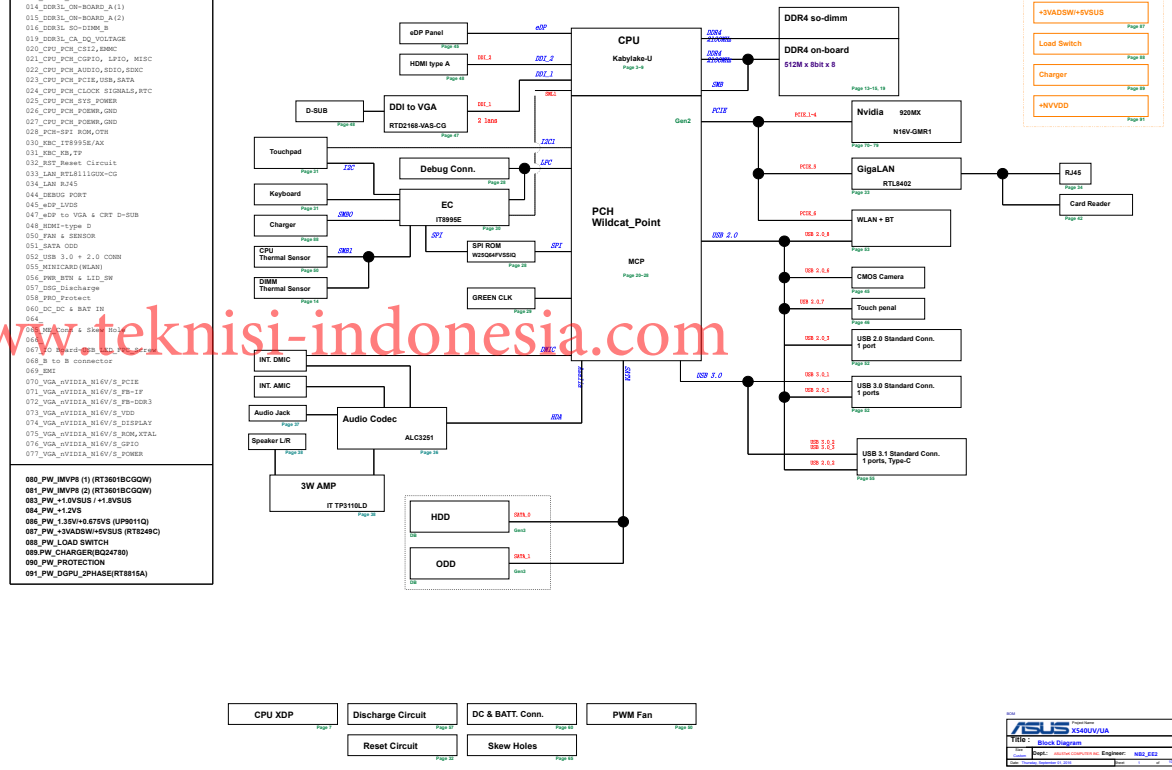
PAGE	Content
001	Block Diagram
002	System Setting
003	CPU_DISPLAY
004	CPU_DDR3
005	CPU_LPC,SPI,SMB,CLINK
006	CPU_POEWR
008	CPU_MISC,JTAG
009	CPU_CFG,RSVD
010	CPU_POWER_CAP
013	DDR3L_TERMINATION
014	DDR3L_ON-BOARD_A(1)
015	DDR3L_ON-BOARD_A(2)
016	DDR3L_SO-DIMM_B
019	DDR3L_CA_DQ_VOLTAGE
020	CPU_PCH_CSI2,EMMC
021	CPU_PCH_CGPIO, LPIO, MISC
022	CPU_PCH_AUDIO,SDIO,SDXC
023	CPU_PCH_PCIE,USB,SATA
024	CPU_PCH_CLOCK SIGNALS,RTC
025	CPU_PCH_SYS_POWER
026	CPU_PCH_POEWR,GND
027	CPU_PCH_POEWR,GND
028	PCH-SPI ROM,OTH
030	KBC_ITE8995E/AX
031	KBC_KB,TP
032	RST_Reset Circuit
033	LAN_RTL8111GUX-CG
034	LAN_RJ45
044	DEBUG PORT
045	eDP_LVDS
047	eDP to VGA & CRT D-SUB
048	HDMI-type D
050	FAN & SENSOR
051	SATA ODD
052	USB 3.0 + 2.0 CONN
055	MINICARD(WLAN)
056	PWR_BTN & LID_SW
057	DSG_Discharge
058	PRO_Protect
060	DC_DC & BAT IN
064	
065	DMIC Conn & Skew Hole
066	
067	I/O Board-USB LED,FAN,Screw
068	B to B connector
069	EMI
070	VGA_nVIDIA_N16V/S_PCIE
071	VGA_nVIDIA_N16V/S_FB-IF
072	VGA_nVIDIA_N16V/S_FB-DDR3
073	VGA_nVIDIA_N16V/S_VDD
074	VGA_nVIDIA_N16V/S_DISPLAY
075	VGA_nVIDIA_N16V/S_ROM,XTAL
076	VGA_nVIDIA_N16V/S_GPIO
077	VGA_nVIDIA_N16V/S_POWER
080	PW_IMVP8 (1) (RT3601BCGQW)
081	PW_IMVP8 (2) (RT3601BCGQW)
083	PW_+1.0VSUS / +1.8VSUS
084	PW_+1.2VS
086	PW_1.35V/+0.675VS (UP9511Q)
087	PW_+3VADSW/+5VSUS (RTB249C)
088	PW_LOAD SWITCH
089	PW_CHARGER(BQ24780)
090	PW_PROTECTION
091	PW_DGPU_2PHASE(RT8815A)

BLOCK DIAGRAM

X541UAK/UVK SCHEMATIC Revision 1.1

(UAK : UMA)
(UVK : DGPU = Nvidia N16V-GMR1, 920MX)

Non Connected Standby



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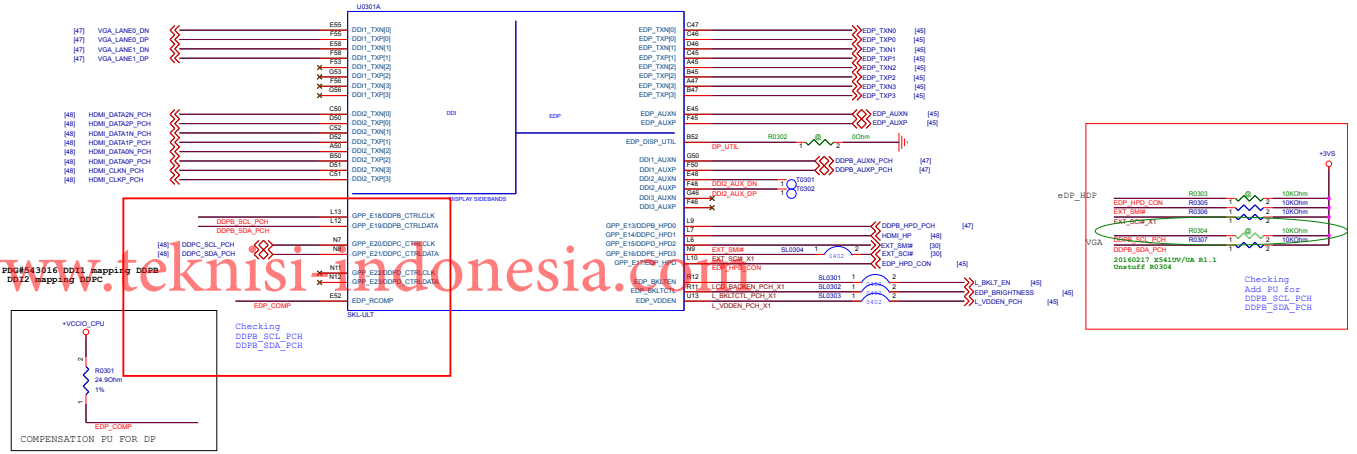
  - 002_System Setting
  - 003_CPU_DISPLAY
  - 004_CPU_DDR4
  - 005_CPU_LPC,SPI,SMB,CLINK
  - 006_CPU_POEWR
  - 007_***
  - 008_CPU_MISC,JTAG
  - 009_CPU_CFG,RSVD
  - 010_CPU_POWER_CAP
  - 011_NB_****
  - 012_NB_****
  - 013_DDR4_TERMINATION_A
  - 014_DDR4_ON-BOARD_A_L32
  - 015_DDR4_ON-BOARD_A_H32
  - 016_DDR4_****
  - 017_DDR4_SO-DIMM_1
  - 018.DDR4_CA VOLTAGE
  - 019_DDR4_****
  - 020_CPU_PCH_CSI2,EMMC
  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC

Main Board

Display Port	
A	EDP
B	VGA
C	HDMI

Intel Version	ASUS P/N
pre-ES	



BOM

ASUS	Project Name: X540UV/UA	Rev: R1.0
Title : CPU_DISPLAY		
Size: Custom	Dept.: ASUSTeK COMPUTER INC	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet 3 of 102	

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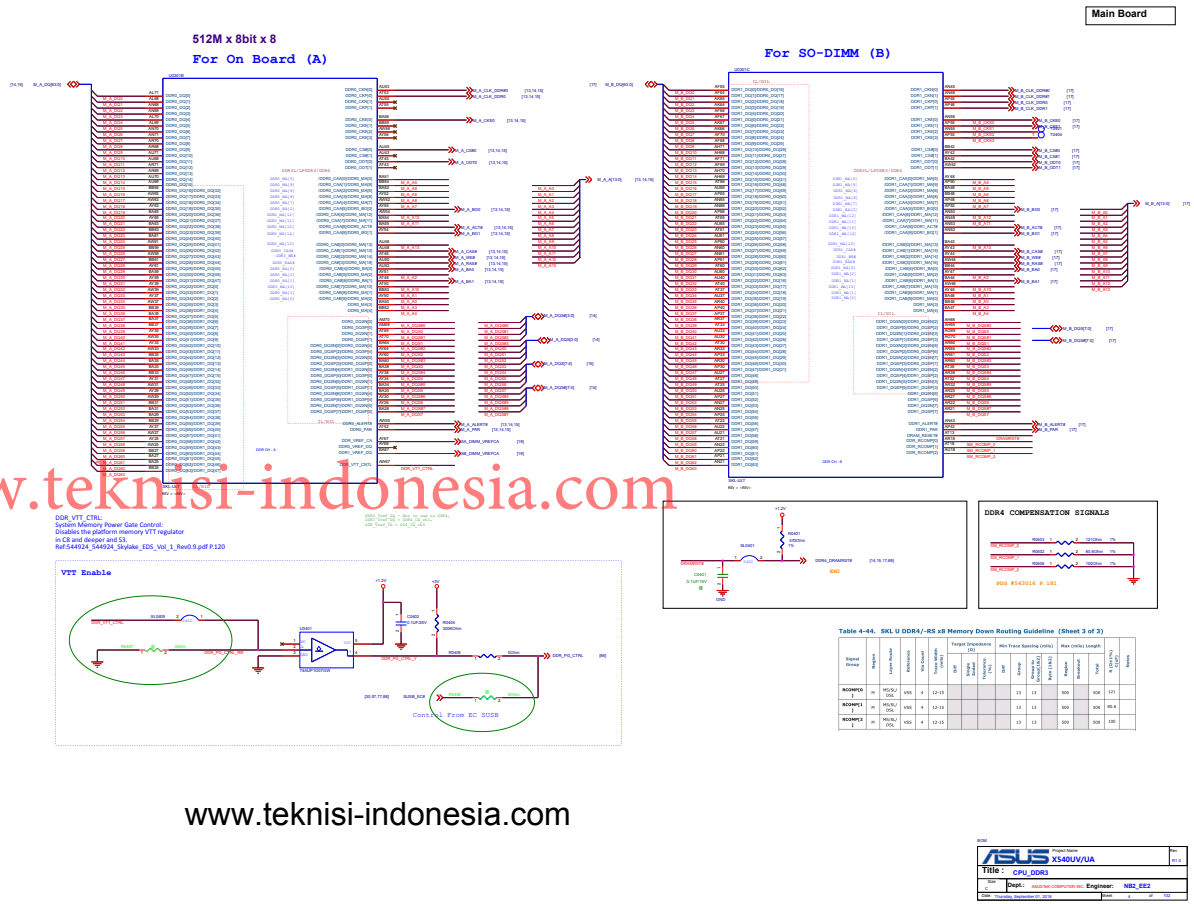

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  - 004_CPU_DDR4
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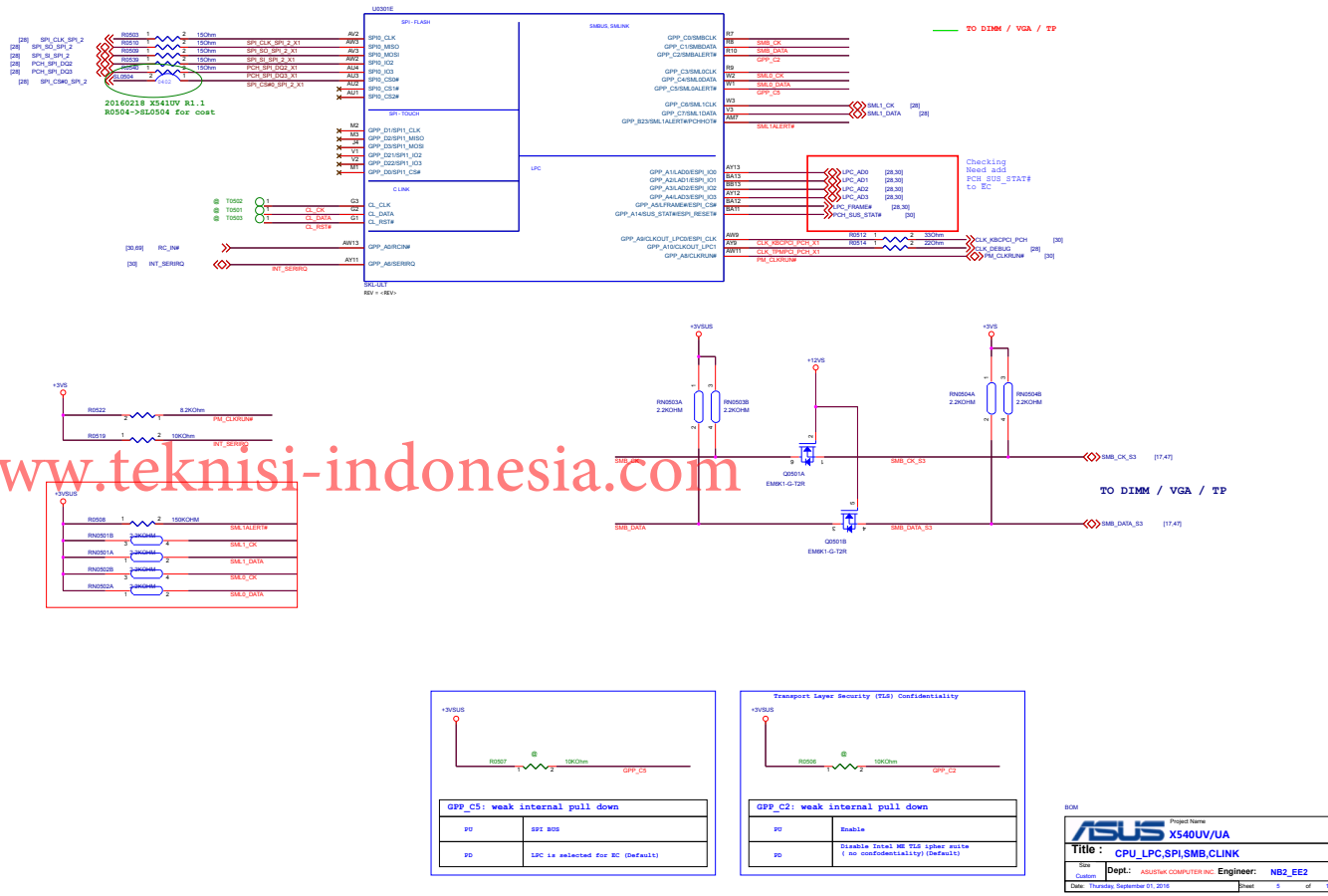
  - 006_CPU_POEWR
  - 007_***
  - 008_CPU_MISC,JTAG
  - 009_CPU_CFG,RSVD
  - 010_CPU_POWER_CAP
  - 011_NB_****
  - 012_NB_****
  - 013_DDR4_TERMINATION_A
  - 014_DDR4_ON-BOARD_A_L32
  - 015_DDR4_ON-BOARD_A_H32
  - 016_DDR4_****
  - 017_DDR4_SO-DIMM_1
  - 018.DDR4_CA VOLTAGE
  - 019_DDR4_****
  - 020_CPU_PCH_CSI2,EMMC
  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC

Global Search | 001 | 002 | 003 | 004 | 005 | 006 | 008 | 009 | 010 | 013 | 014

Toggle FullScreen | Pre Page | Next Page | MoveTo

Main Board



Project Name	X540UV/UA
Rev	R1.0
Title :	CPU_LPC,SPI,SMB,CLINK
Size	Custom
Dept.:	ASUSTeK COMPUTER INC
Engineer:	NB2_EE2
Date:	Thursday, September 01, 2016
Sheet	5 of 102

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  - 005_CPU_LPC,SPI,SMB,CLINK
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  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC

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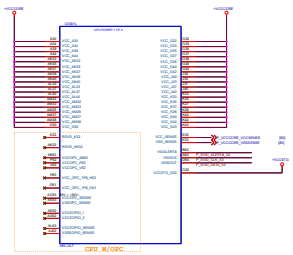

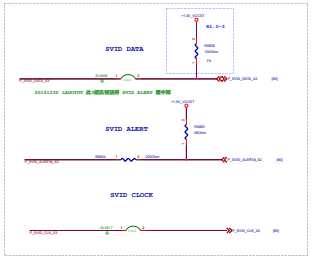

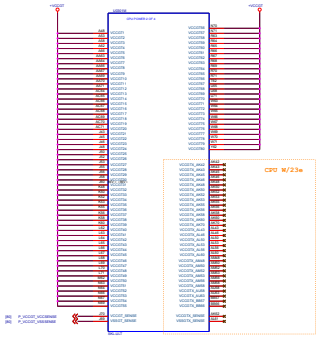

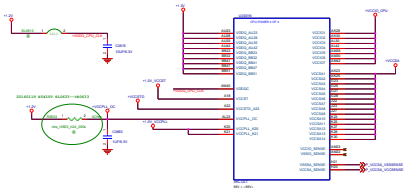

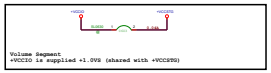

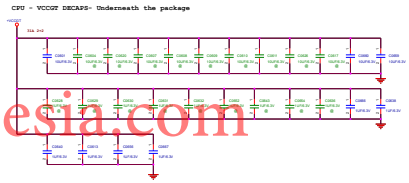

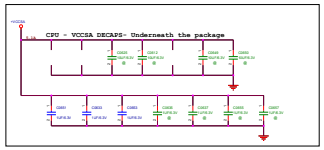

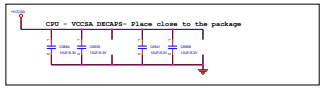

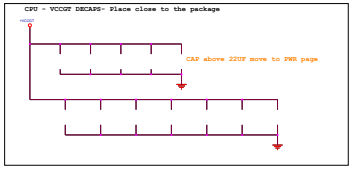

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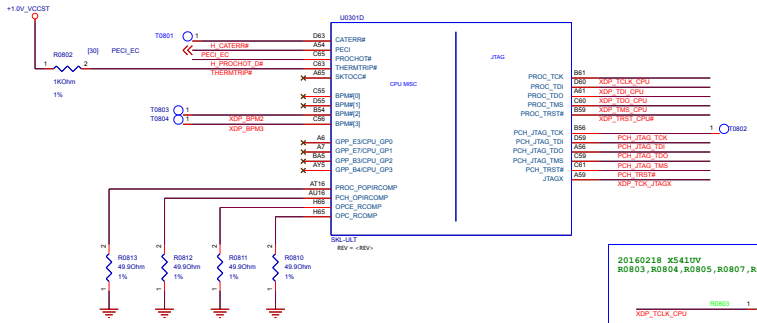
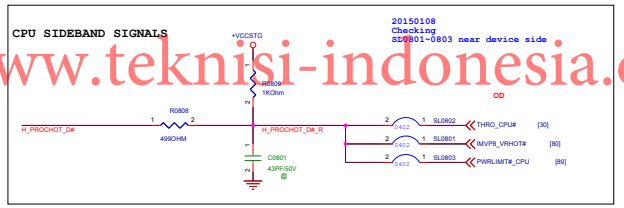
  - 019_DDR4_****
  - 020_CPU_PCH_CSI2,EMMC
  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC

Main Board

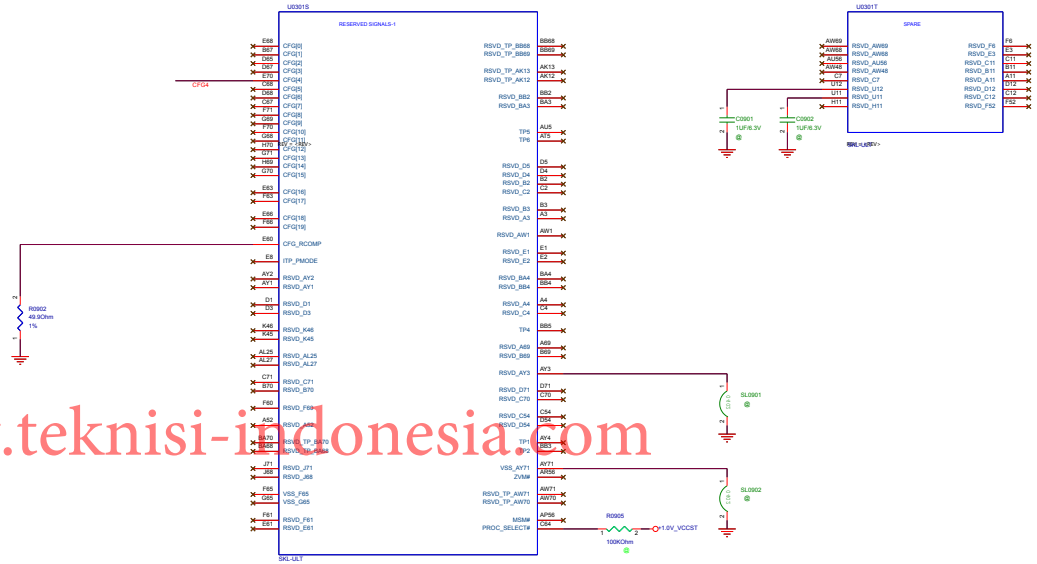


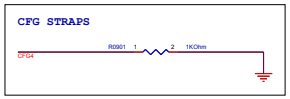


BOM

ASUS	Project Name: X540UV/UA	Rev: R1.0
Title : CPU_MISC,JTAG,CLK		
Size: B	Dept.: ASUSTeK COMPUTER INC. Engineer: NB2_EE2	
Date: Thursday, September 01, 2016	Sheet 8 of 102	

Main Board





	1	0	NOTE
CFG0	NO STALL	STALL	STALL RESET SEQUENCE AFTER PCU PLL LOCK UNTIL DE-ASSERTED
CFG4	DISABLE	ENABLE	eDP ENABLE

BOM

ASUS Project Name: X540UV/UA Rev: R1.0

Title : CPU_CFG,RSVD

Size: Custom | Dept.: ASUSTeK COMPUTER INC. | Engineer: NB2_EE2

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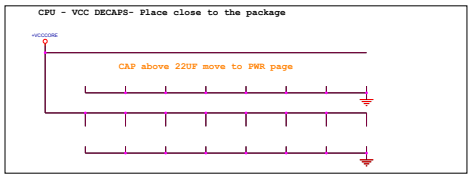
  - 006_CPU_POEWR
  - 007_***
  - 008_CPU_MISC,JTAG
  - 009_CPU_CFG,RSVD
  - 010_CPU_POWER_CAP
  - 011_NB_****
  - 012_NB_****
  - 013_DDR4_TERMINATION_A
  - 014_DDR4_ON-BOARD_A_L32
  - 015_DDR4_ON-BOARD_A_H32
  - 016_DDR4_****
  - 017_DDR4_SO-DIMM_1
  - 018.DDR4_CA VOLTAGE
  - 019_DDR4_****
  - 020_CPU_PCH_CSI2,EMMC
  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC



BOM

ASUS Project Name: X540UV/UA

Title : CPU_POWER_CAP

Dept.: Engineer: NB2_EE2

Date: Thursday, September 01, 2016

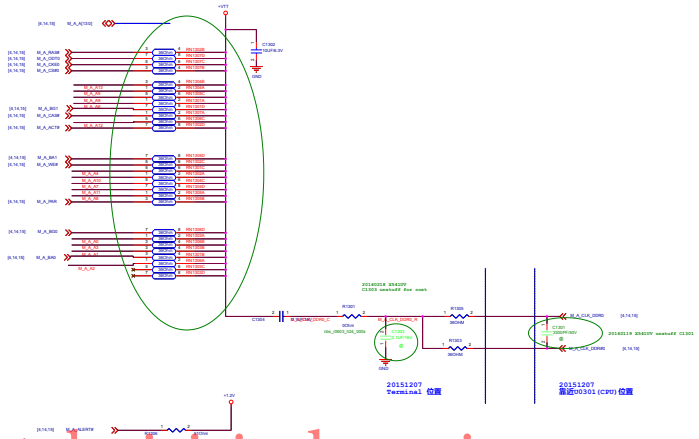


Table 4-2. System Memory Interface Guideline Terminology and Descriptions

SKL Processor and Memory Type	SKL H			
	DDR4/-RS SO-DIMM+ECC	DDR4/-RS SO-DIMM no ECC	DDR4/-RS Memory Down	LPDDR3 Memory Down
Signal Group Details				
Clock (CLK)	CKN[3:0], CKP[3:0]	CKN[3:0], CKP[3:0]	CKN[1:0], CKP[1:0]	CKP[1:0], CKN[1:0]
Control (CTRL)	CS#[3:0], ODT[3:0]	CS#[3:0], ODT[3:0]	CS#[1:0], ODT[1:0]	CS#[1:0], ODT[0]
Clock Enable (CKE)	CKE[3:0]	CKE[3:0]	CKE[1:0]	CKE[3:0]
Command (CMD)	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	MA[16:0], BG[1:0], BA[1:0],ACT#, PAR	MA[16:0], BG[1:0], BA[1:0], ACT#, PAR	CAA[9:0], CAB[9:0]
Strobe	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQSP[7:0], DQSN[7:0]	DQS[7:0], DQS#[7:0]
ECC strobe	DQSP[8], DQSN[8]	N/A	N/A	N/A
Data	DQ[63:0]	DQ[63:0]	DQ[63:0]	DQ[63:0]
ECC Data	DQ[71:64]	N/A	N/A	N/A
Alert	ALERT#	ALERT#	ALERT#	N/A
Reset	DRAM_RESET#	DRAM_RESET#	DRAM_RESET#	N/A
RCOMP	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]	DDR_RCOMP[2:0]

ASUS Title : DDR4_TERMINATION_A
Engineer: NB2_EE2
Project Name: X540UV/UA

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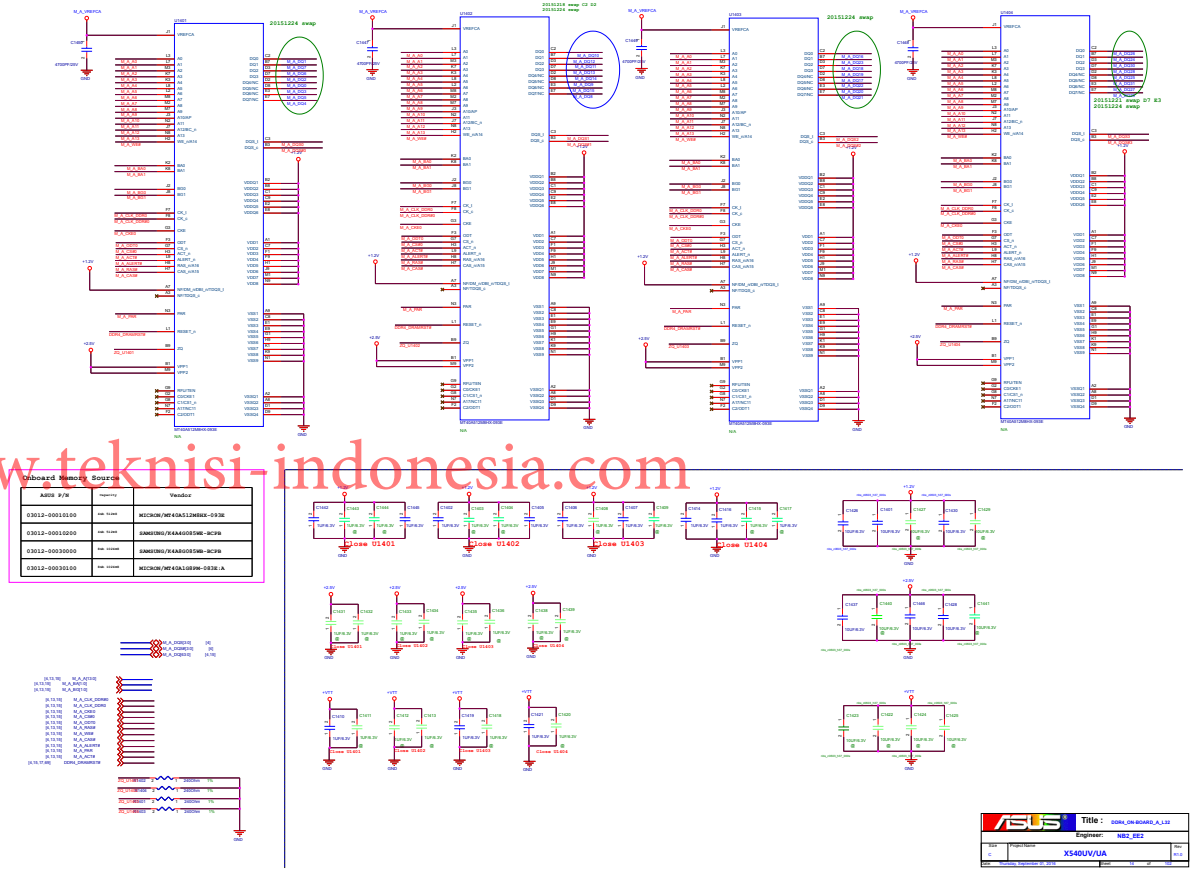
  - 005_CPU_LPC,SPI,SMB,CLINK
  - 006_CPU_POEWR
  - 007_***
  - 008_CPU_MISC,JTAG
  - 009_CPU_CFG,RSVD
  - 010_CPU_POWER_CAP
  - 011_NB_****
  - 012_NB_****
  - 013_DDR4_TERMINATION_A
  - 014_DDR4_ON-BOARD_A_L32
  - 015_DDR4_ON-BOARD_A_H32
  - 016_DDR4_****
  - 017_DDR4_SO-DIMM_1
  - 018.DDR4_CA VOLTAGE
  - 019_DDR4_****
  - 020_CPU_PCH_CSI2,EMMC
  - 021_CPU_PCH_CGPIO, LPIO, MISC
  - 022_CPU_PCH_AUDIO,SDIO,SDXC



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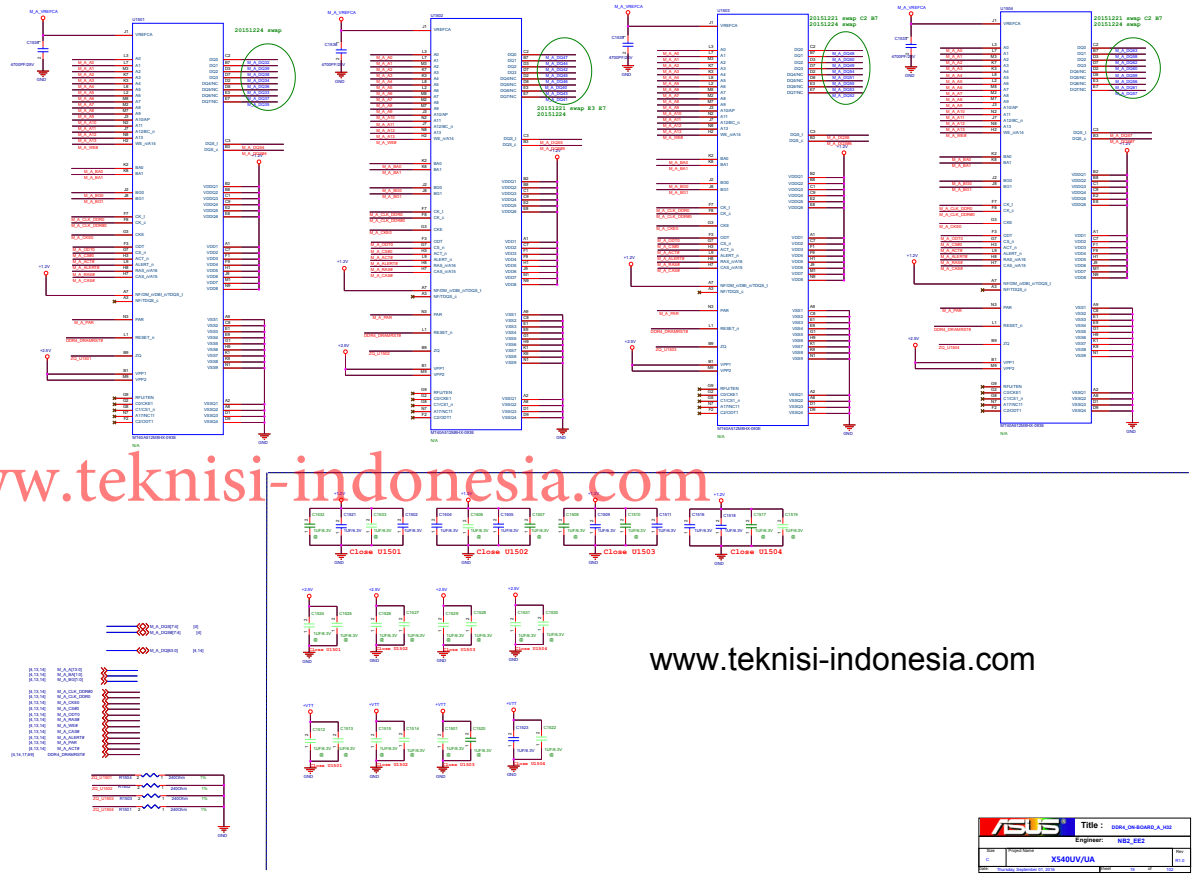
018.DDR4_CA VOLTAGE
019_DDR4_****
020_CPU_PCH_CSI2,EMMC
021_CPU_PCH_CGPIO, LPIO, MISC
022_CPU_PCH_AUDIO,SDIO,SDXC

023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNALS,RTC
025_CPU_PCH_SYS_POWER
026_CPU_PCH_POEWR,GND
027_CPU_PCH_POEWR,GND
028_PCH-SPI ROM,OTH,DEBUG
029. Silego_Green_CLK_Gen___
030_IT8995E-128/CX
031_KBC_KB,TP,KB-light
032_RST_Reset Circuit
033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
040



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- 018.DDR4_CA VOLTAGE
- 019_DDR4_****
- 020_CPU_PCH_CSI2,EMMC
- 021_CPU_PCH_CGPIO, LPIO, MISC
- 022_CPU_PCH_AUDIO,SDIO,SDXC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNALS,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040

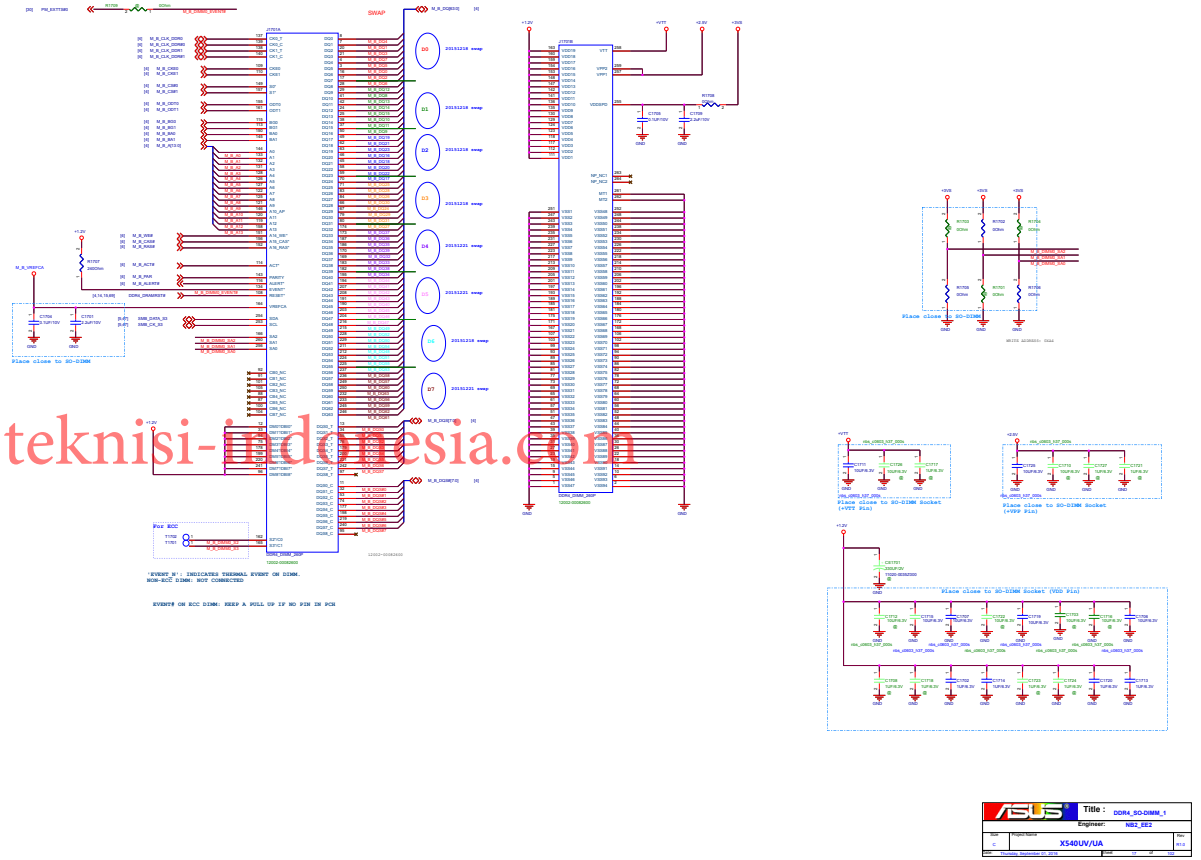


Figure 4-51. SKL U DDR4/-RS x8 Devices Memory Down V_{REF-CA} Overview

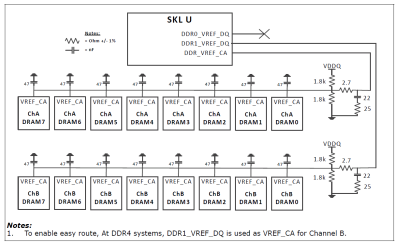
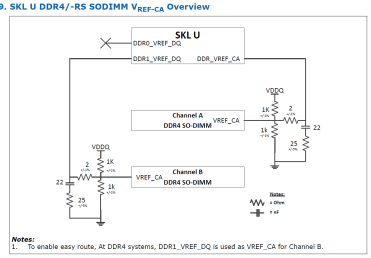
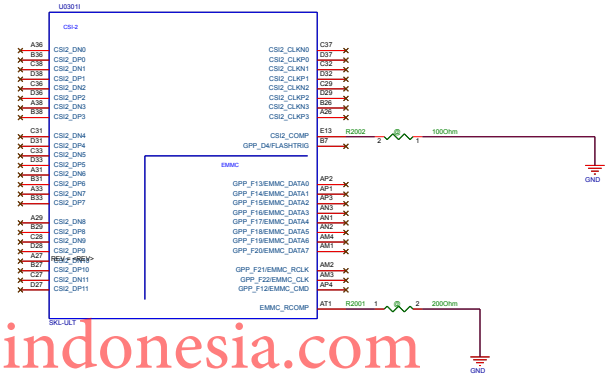


Figure 4-49. SKL U DDR4/-RS SODIMM V_{REF-CA} Overview



All Vref trace must be 20 mils width

Title : DDR4 CA VOLTAGE
Engineer: N82_EE2
X540UV/UA



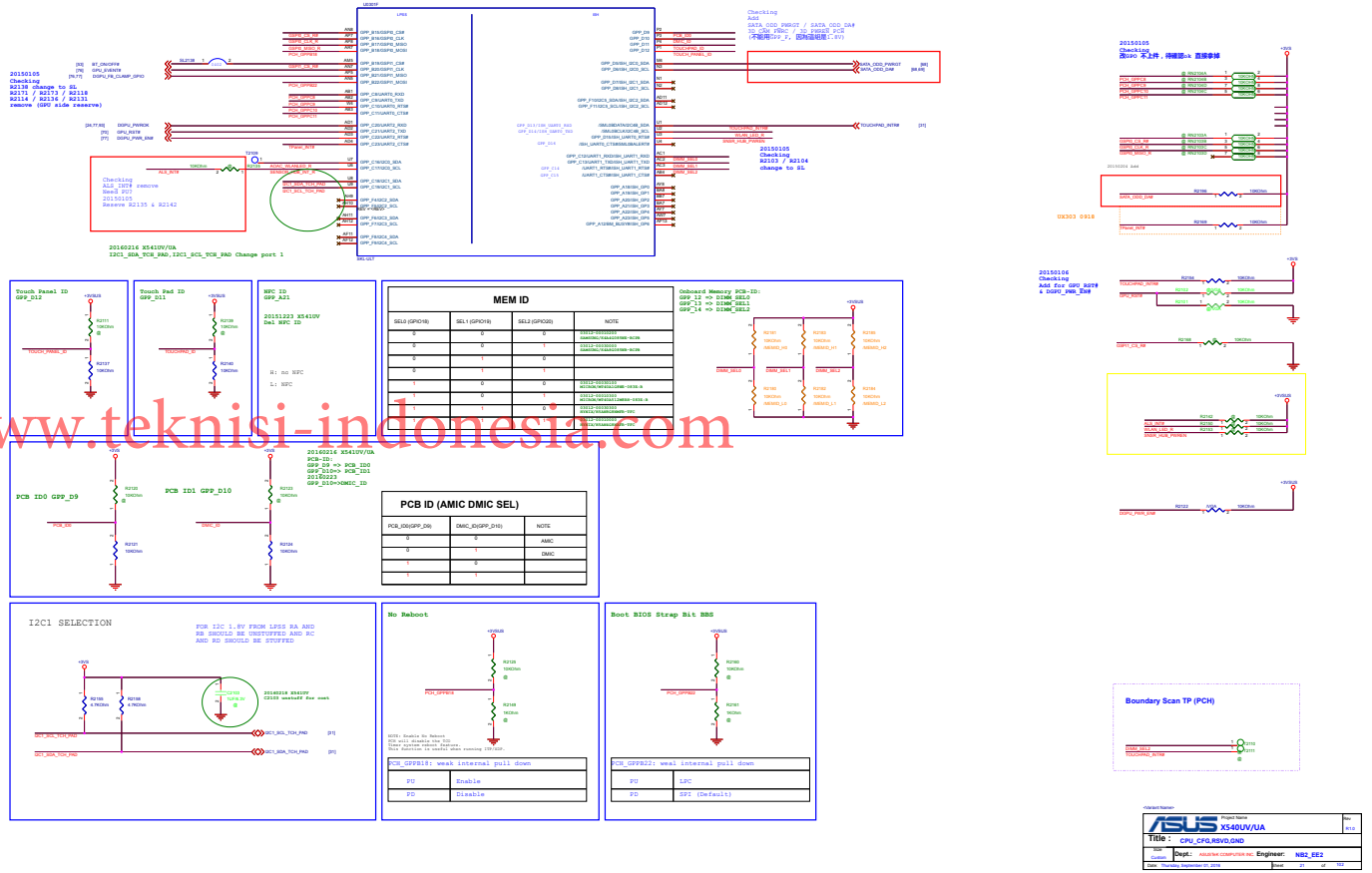
BOM

ASUS	Project Name: X540UV/UA	Rev: R1.0
Title :	CPU_PCH_CSI2,EMMC	
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet 20 of 102	

Schematic Page List Hide

018.DDR4_CA VOLTAGE
019_DDR4_****
020_CPU_PCH_CSI2,EMMC
021_CPU_PCH_CGPIO, LPIO, MISC
022_CPU_PCH_AUDIO,SDIO,SDXC
023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNALS,RTC
025_CPU_PCH_SYS_POWER
026_CPU_PCH_POEWR,GND
027_CPU_PCH_POEWR,GND
028_PCH-SPI ROM,OTH,DEBUG
029. Silego_Green_CLK_Gen___
030_IT8995E-128/CX
031_KBC_KB,TP,KB-light
032_RST_Reset Circuit
033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
040

Main Board



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018.DDR4_CA VOLTAGE
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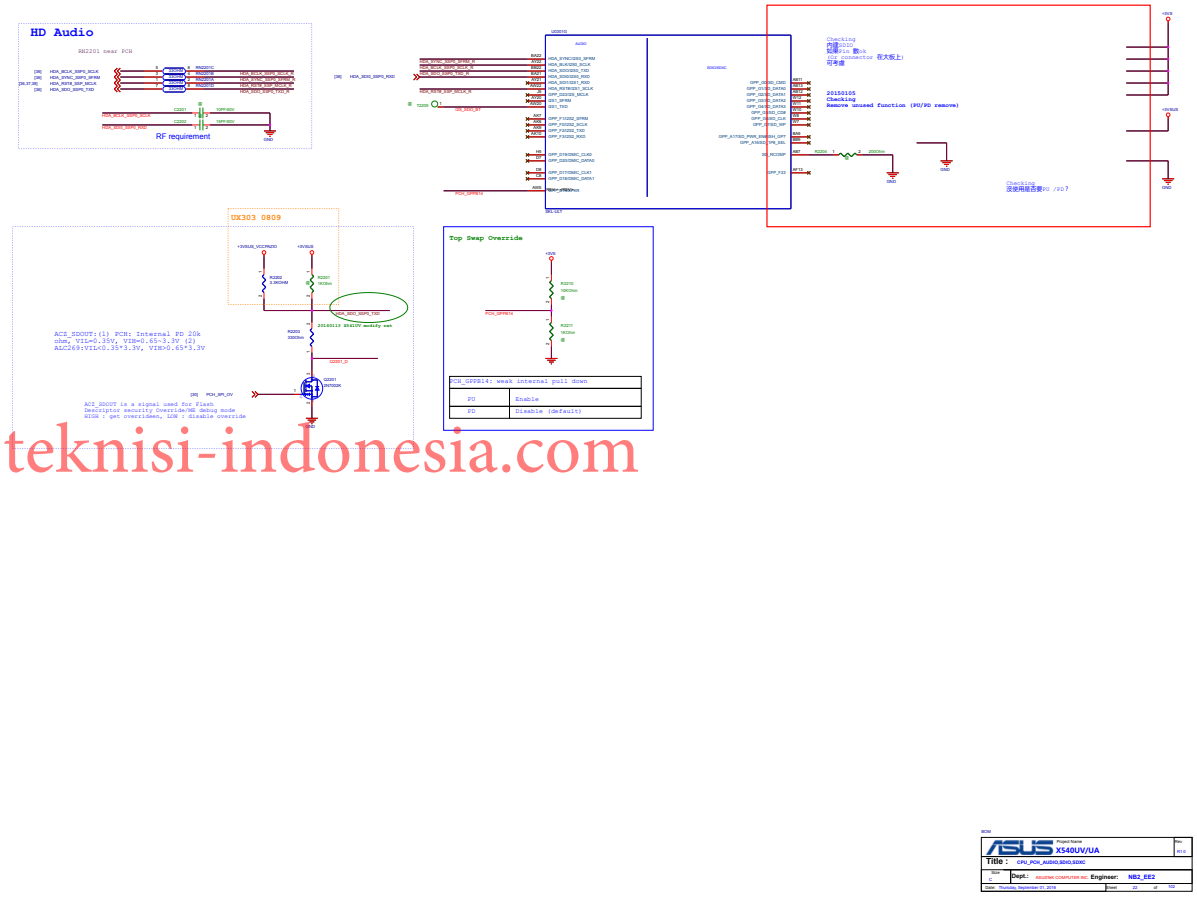
023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNALS,RTC
025_CPU_PCH_SYS_POWER
026_CPU_PCH_POEWR,GND
027_CPU_PCH_POEWR,GND
028_PCH-SPI ROM,OTH,DEBUG
029. Silego_Green_CLK_Gen___
030_IT8995E-128/CX
031_KBC_KB,TP,KB-light
032_RST_Reset Circuit
033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
040



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018.DDR4_CA VOLTAGE
019_DDR4_****
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021_CPU_PCH_CGPIO, LPIO, MISC
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023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNALS,RTC
025_CPU_PCH_SYS_POWER
026_CPU_PCH_POEWR,GND
027_CPU_PCH_POEWR,GND
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033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
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Global Search | 015 | 017 | 018 | 020 | 021 | 022 | 023 | 024 | 025 | 026 | 027

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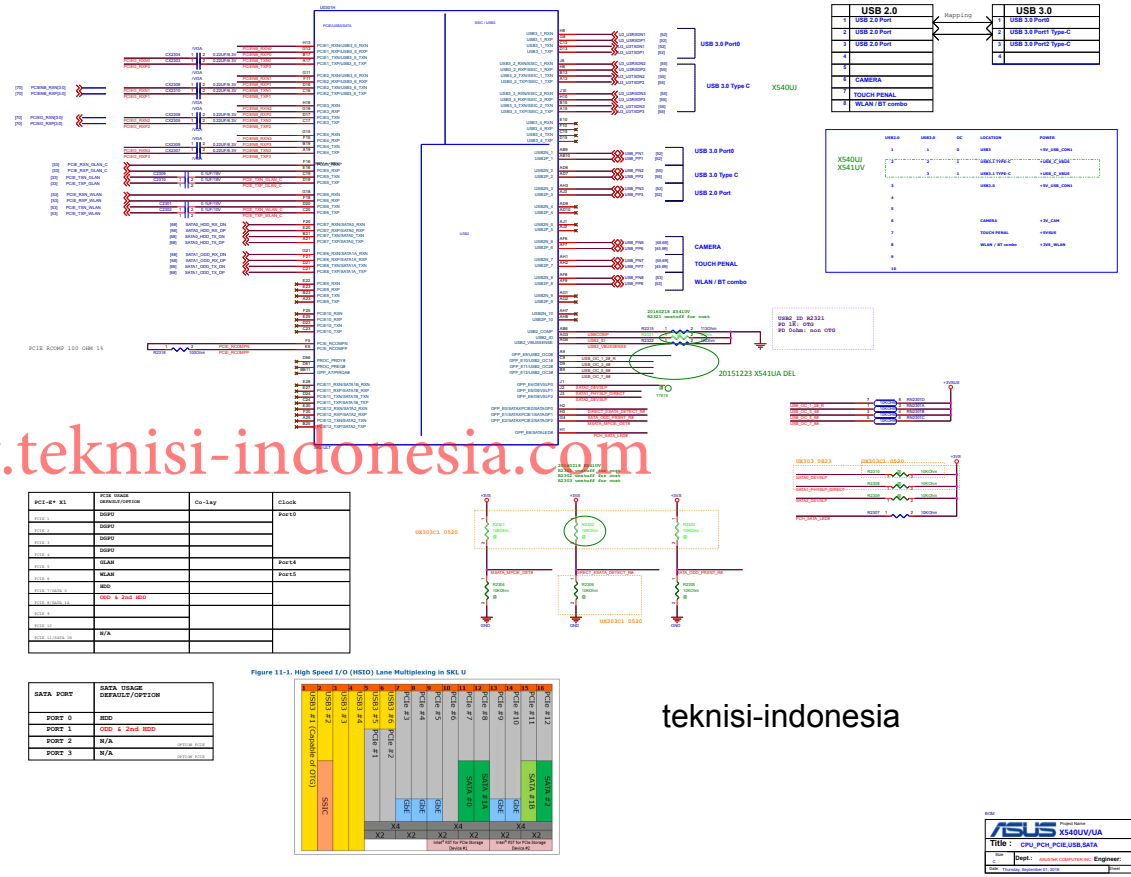

PCI-E* X1	PCIE USAGE DEFAULT/OPTION	Co-lay	Clock
	DGPU		Port0
	DGPU		
	DGPU		
	DGPU		
	GLAN		Port4
	WLAN		Port5
	HDD		
	ODD & 2nd HDD		
	N/A		

SATA PORT	SATA USAGE DEFAULT/OPTION
PORT 0	HDD
PORT 1	ODD & 2nd HDD
PORT 2	N/A
PORT 3	N/A

Figure 11-1. High Speed I/O (HSIO) Lane Multiplexing in SKL U

Schematic Page List Hide

018.DDR4_CA VOLTAGE
019_DDR4_****
020_CPU_PCH_CSI2,EMMC
021_CPU_PCH_CGPIO, LPIO, MISC
022_CPU_PCH_AUDIO,SDIO,SDXC

023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNALS,RTC
025_CPU_PCH_SYS_POWER
026_CPU_PCH_POEWR,GND
027_CPU_PCH_POEWR,GND
028_PCH-SPI ROM,OTH,DEBUG
029. Silego_Green_CLK_Gen___
030_IT8995E-128/CX
031_KBC_KB,TP,KB-light
032_RST_Reset Circuit
033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
040

Global Search | 015 | 017 | 018 | 020 | 021 | 022 | 023 | 024 | 025 | 026 | 027

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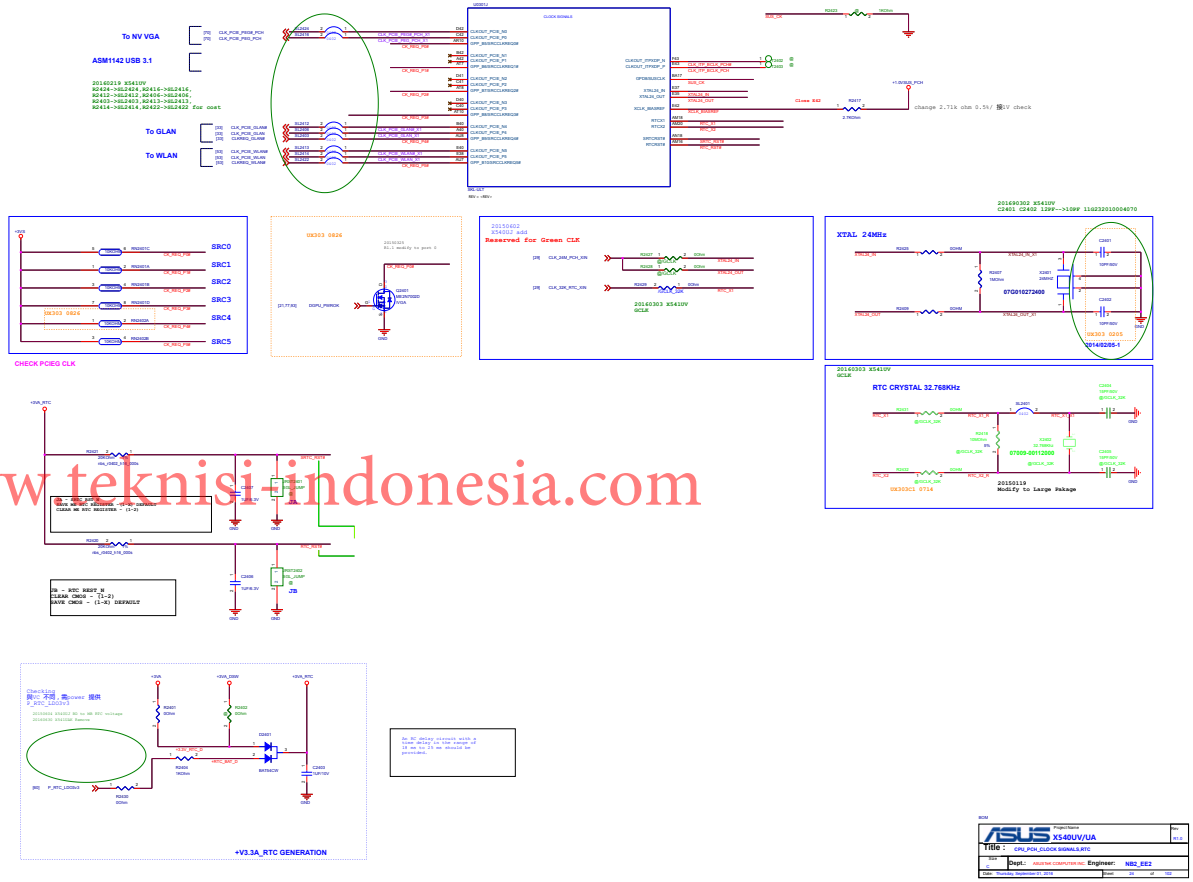

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- 022_CPU_PCH_AUDIO,SDIO,SDXC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNALS,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040

Global Search | 015 | 017 | 018 | 020 | 021 | 022 | 023 | 024 | 025 | 026 | 027

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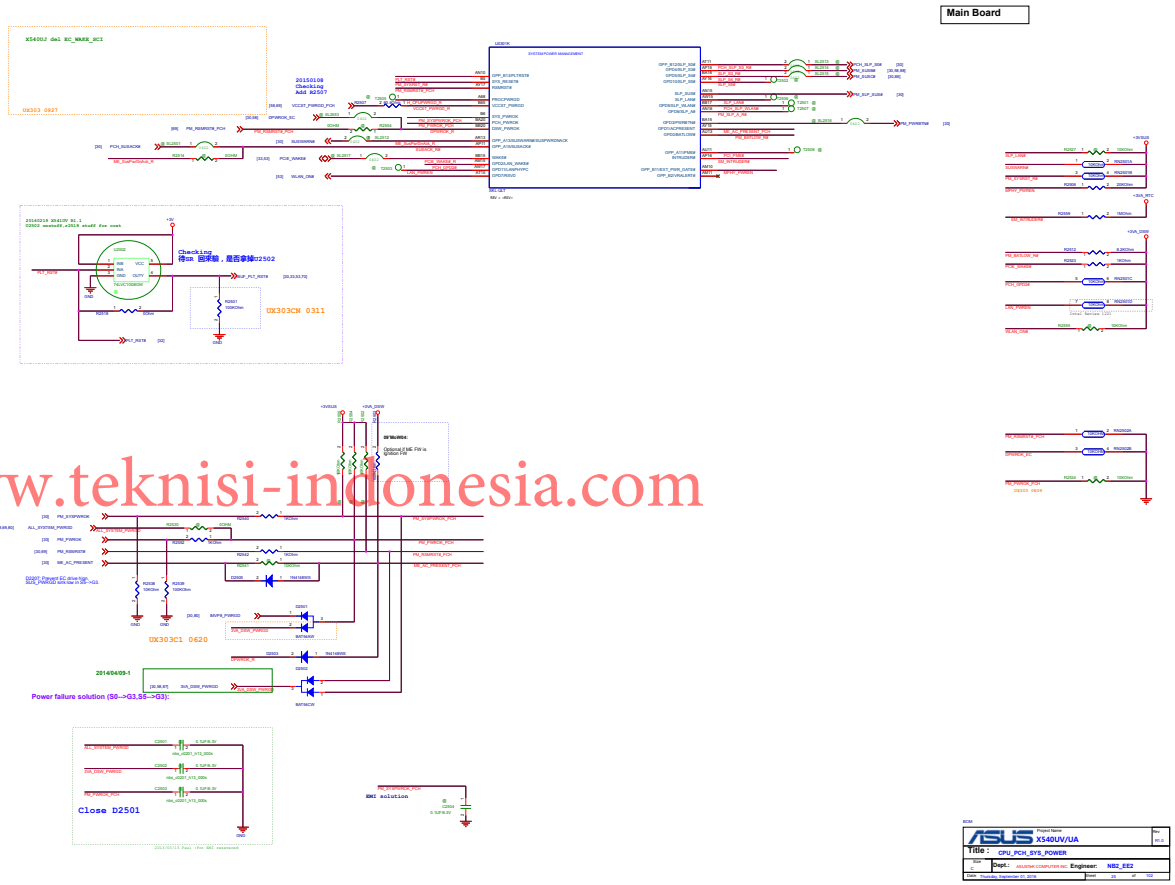

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- 018.DDR4_CA VOLTAGE
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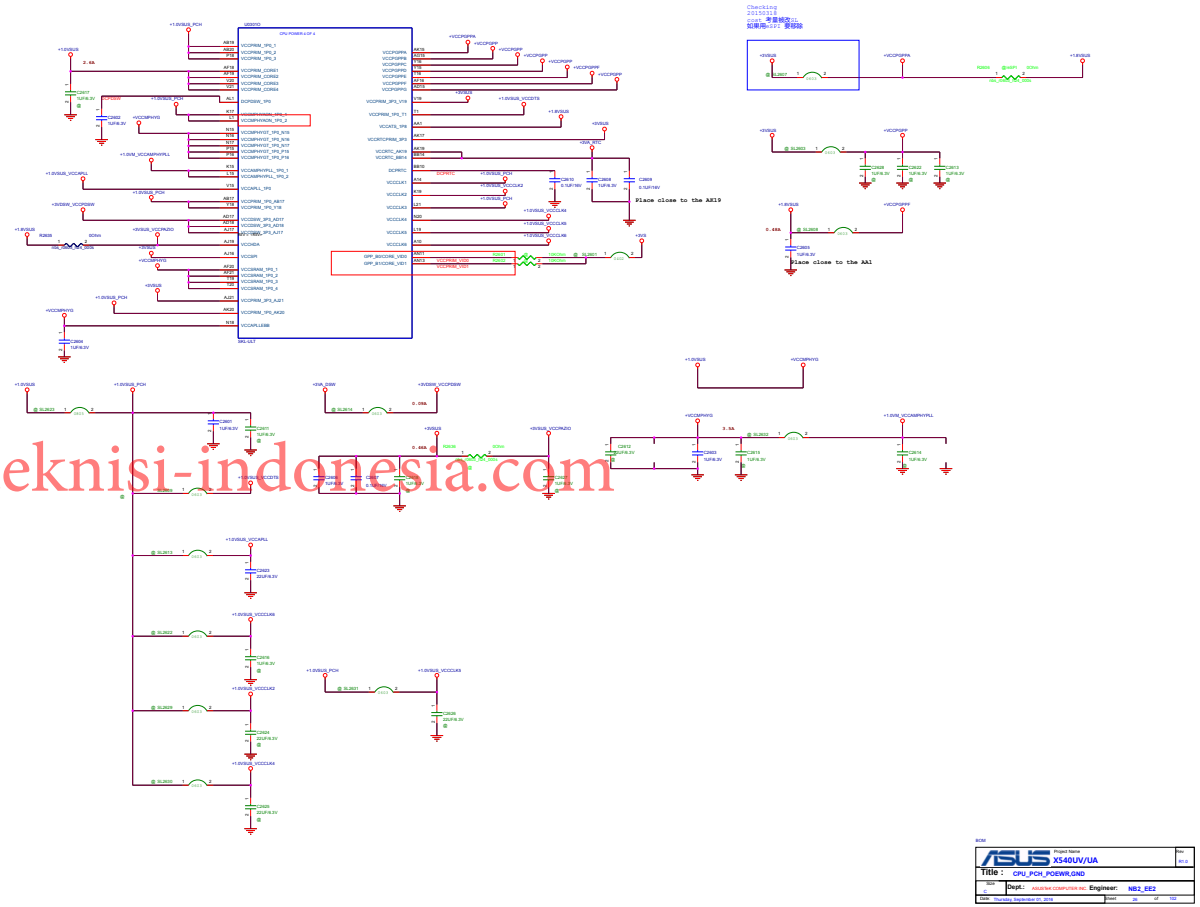
- 021_CPU_PCH_CGPIO, LPIO, MISC
- 022_CPU_PCH_AUDIO,SDIO,SDXC
- 023_CPU_PCH_PCIE,USB,SATA
- 024_CPU_PCH_CLOCK SIGNALS,RTC
- 025_CPU_PCH_SYS_POWER
- 026_CPU_PCH_POEWR,GND
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040



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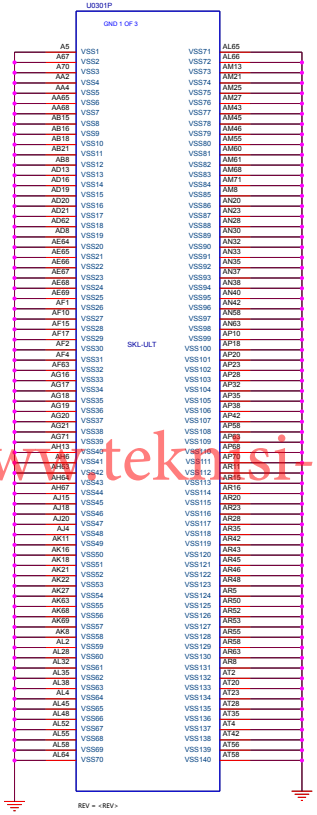
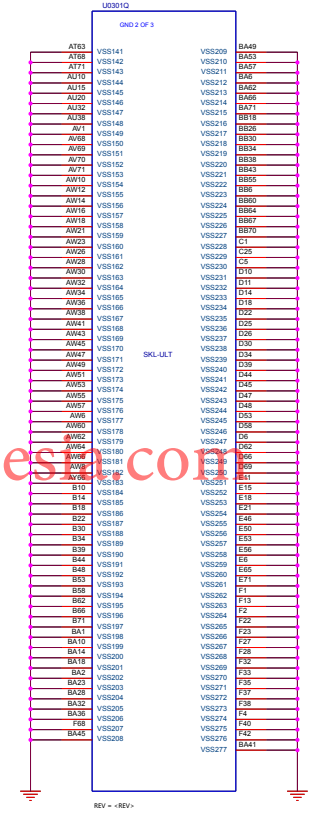
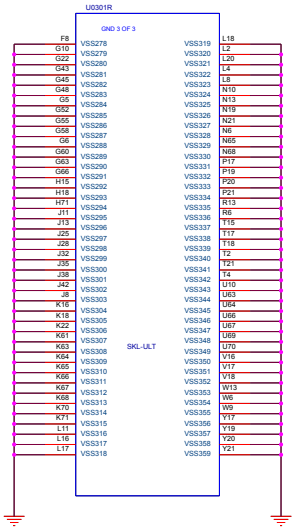
018.DDR4_CA VOLTAGE
019_DDR4_****
020_CPU_PCH_CSI2,EMMC
021_CPU_PCH_CGPIO, LPIO, MISC
022_CPU_PCH_AUDIO,SDIO,SDXC
023_CPU_PCH_PCIE,USB,SATA
024_CPU_PCH_CLOCK SIGNALS,RTC
025_CPU_PCH_SYS_POWER
026_CPU_PCH_POEWR,GND
027_CPU_PCH_POEWR,GND
028_PCH-SPI ROM,OTH,DEBUG
029. Silego_Green_CLK_Gen___
030_IT8995E-128/CX
031_KBC_KB,TP,KB-light
032_RST_Reset Circuit
033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
040







BOM

REV	Project Name: X540UV/UA	Rev: R1.0
Title : CPU_PCH_POEWR,GND		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet 27 of 102	

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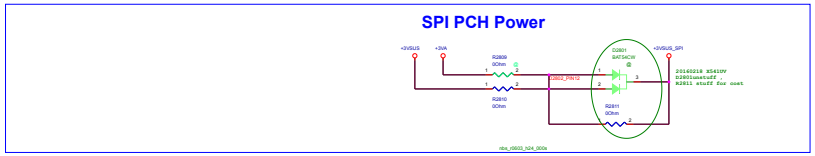
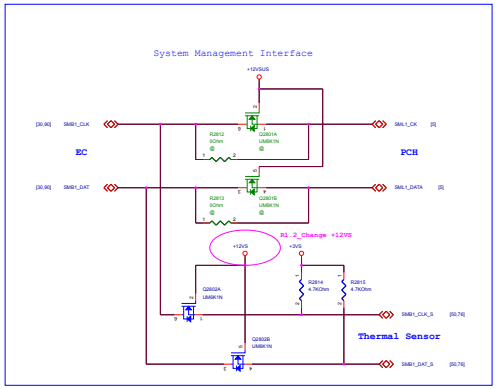
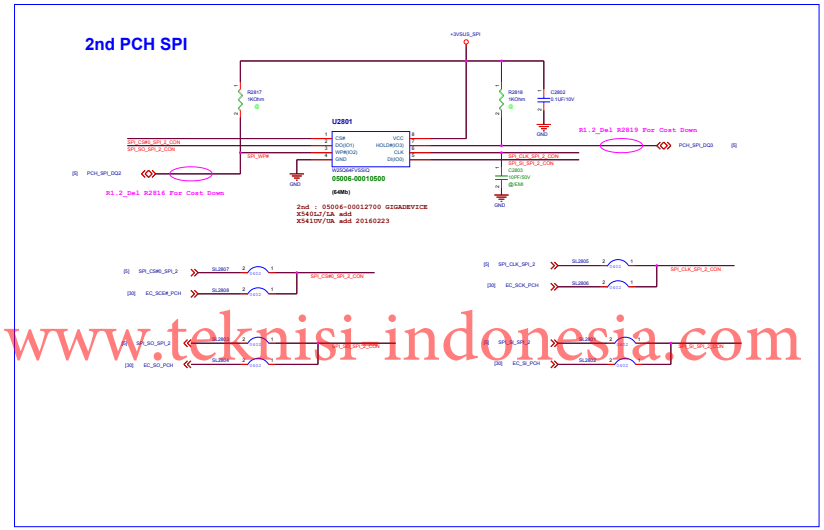
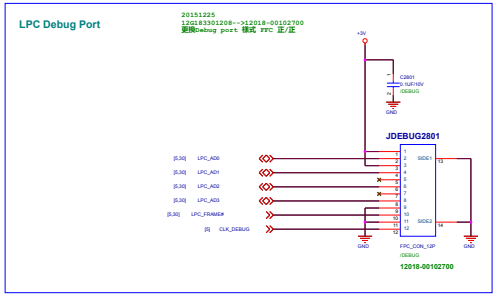
- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTOR
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor



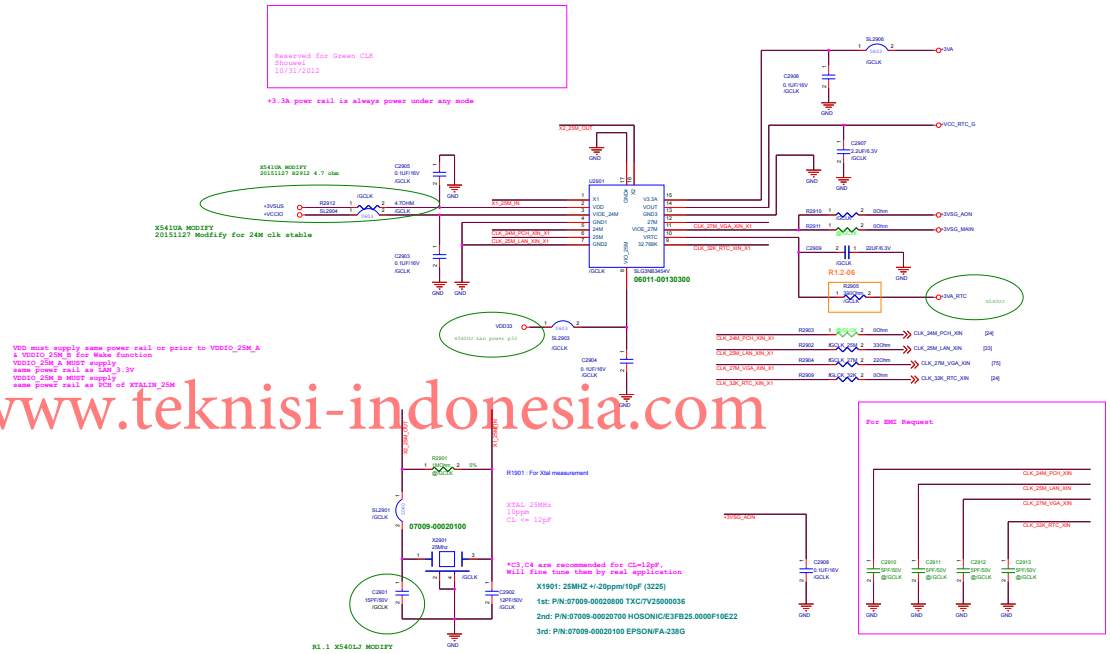






Title : 28_PCH-SPI ROM,OTH
Engineer: NB2_EE2
X540UV/UA

Silego Green CLK



Title :	Green CLK Gen
Engineer:	NB2_EE2
Project Name	X540UV/UA

Schematic Page List Hide

- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTOR
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor

Global Search | 028 | 029 | 030 | 031 | 032 | 033 | 034 | 036 | 037 | 038 | 042

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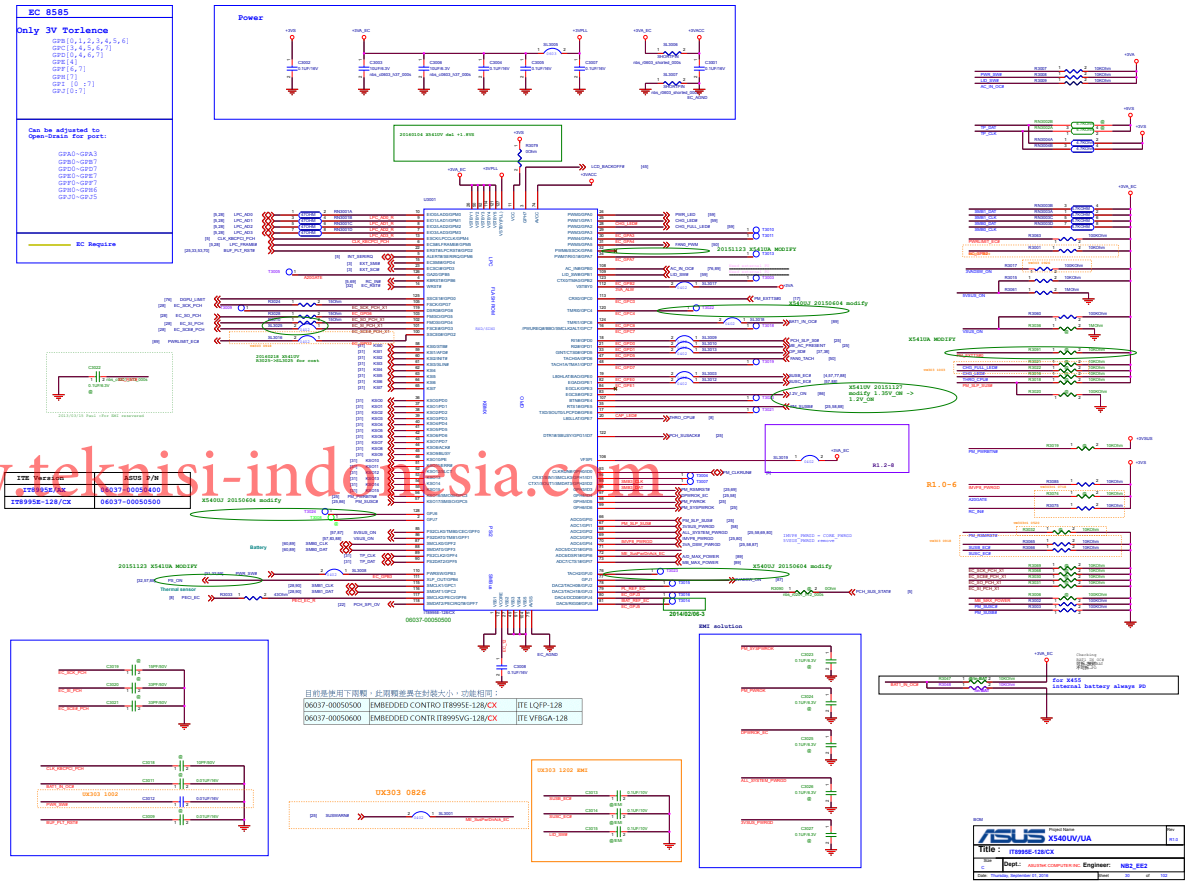
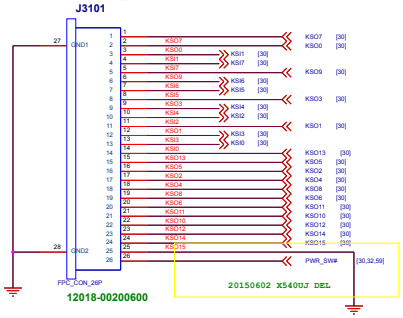
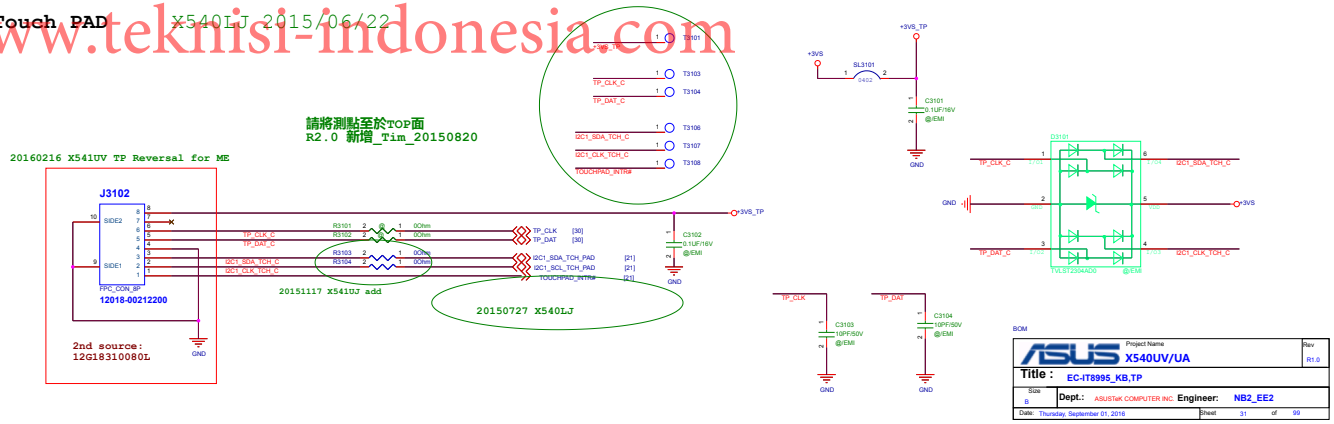


Internal Keyboard

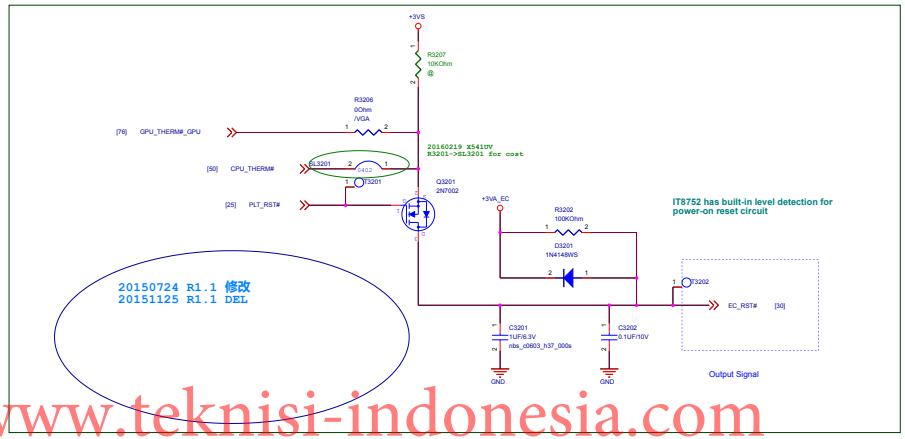


Touch PAD

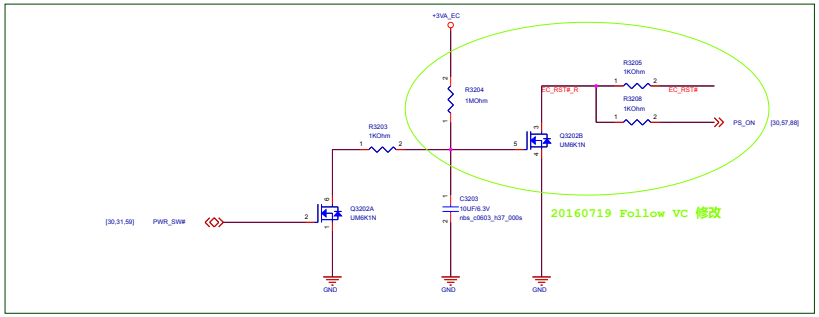
X540LJ 2015/06/22

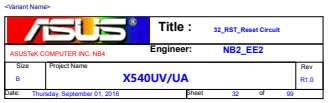


Thermal Policy



battery embedded (press pwr_sw 10sec, then reset ec)





Schematic Page List Hide

5.1. Power Management/Isolation

Table 1. Power Management/Isolation

Symbol	Type	Pin No	Description
LANWAKEB	O/D	53	Power Management Event: Open drain, active low. Used to reactivate the PCI Express slot's main power rails and reference clocks.
ISOLATEB	I	52	Isolate Pin: Active low. Used to isolate the RTL8402 from the PCI Express bus. The RTL8402 will not drive its PCI Express outputs (excluding LANWAKEB) and will not sample its PCI Express input as long as the Isolate pin is asserted.

5.2. PCI Express Interface

Table 2. PCI Express Interface

Symbol	Type	Pin No	Description
REFCLK_P	I	21	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm.
REFCLK_N	I	22	
HSOP	O	23	PCI Express Transmit Differential Pair.
HSON	O	24	
HSIP	I	19	PCI Express Receive Differential Pair.
HSIN	I	20	
PERSTB	I	30	PCI Express Reset Signal: Active low. When the PERSTB is asserted at power-on state, the RTL8402 returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.
CLKREQB	O/D	29	Reference Clock Request Signal. This signal is used by the RTL8402 to request starting of the PCI Express reference clock.

5.3. EEPROM (TWSI)

Table 3. EEPROM (TWSI)

Symbol	Type	Pin No	Description
SCL/LED_CR	O	35	SCL, Clock interface for TWSI EEPROM.
SDA	IO	36	SDA, Data interface for TWSI EEPROM. Refer to the reference schematic for strapping pin information. All strapping pins are power-on latch pins.

5.4. Transceiver Interface

Table 4. Transceiver Interface

Symbol	Type	Pin No	Description
MDIP0	IO	2	In MDI mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
MDIN0	IO	3	In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIP1	IO	4	In MDI mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
MDIN1	IO	5	In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.

5.5. Clock

Table 5. Clock

Symbol	Type	Pin No	Description
CKXTAL1	I	45	Input of 25MHz Clock Reference.
CKXTAL2	IO	46	Output of 25MHz Clock Reference. Input of External Clock Source.

5.6. Reference

Table 6. Reference

Symbol	Type	Pin No	Description
RSET	I	48	Reference. External resistor reference.

5.7. LEDs

Table 7. LEDs

Symbol	Type	Pin No	Description
SCL/LED_CR	O	35	See Section 6.2.5 Customizable LED Configuration, Page 11 for Details.
LED0	O	39	
LED1	O	37	

Note: During power down mode, the LED signals are logic high.

5.8. Card Reader

Table 8. Card Reader

Symbol	Type	Pin No	Description
SD_D0/MS_D7/xD_D5	IO	13	SD Data 0 (SD_DAT0), MS_Data 7 (MS_D7), and xD Data 5 (xD_D5).
SD_D1/MS_CLK/xD_D6	IO	12	SD Data 1 (SD_DAT1), MS Clock (MS_CLK), and xD Data 6 (xD_D6).
SD_D2/xD_D7	IO	17	SD Data 2 (SD_DAT2) and xD Data 7 (xD_D7).
SD_D3/MS_D3/xD_D1	IO	16	SD Data 3 (SD_DAT3), MS_Data 2 (MS_D2), and xD Data 2 (xD_D3).
SD_D4/xD_WE#	IO	11	SD Data 4 (SD_DAT4) and xD Write Enable (xD_WE#).
SD_D5/xD_CE#	IO	10	SD Data 5 (SD_DAT5) and xD Chip Select (xD_CE#).
SD_D6/MS_INS#/xD_RE#	IO	9	SD Data 6 (SD_DAT6), MS Card Detect (MS_INS#), and xD Read Enable (xD_RE#).
SD_D7/xD_RDY	IO	8	SD Data 7 (SD_DAT7) and xD Ready Signal (xD_RDY).
SD_CLK/MS_D3/xD_D4	IO	14	SD Clock (SD_CLK), MS_Data 3 (MS_D3), and xD Data 4 (xD_D4).
SD_CMD/MS_D6/xD_D3	IO	15	SD Serial Protocol Command, and Response Signal, MS_Data 6 (MS_D6), and xD Data 3 (xD_D3).
SD_WP/MS_D1/xD_WP#	IO	28	SD Write Protect (SD_WP), MS_Data 1 (MS_D1), and xD Write Protect (xD_WP#).
SD_CD#/MS_D5/xD_ALE	IO	41	SD Card Detect (SD_CD#), MS_Data 5 (MS_D5), and xD Address Latch Enable (xD_ALE).
MS_BS/xD_CLE	IO	27	MS_BS and xD Command Latch Enable (xD_CLE).
MS_D4/xD_D0	IO	42	MS_Data 4 (MS_D4) and xD Data 0 (xD_D0).
MS_D0/xD_D1	IO	43	MS_Data 0 (MS_D0) and xD Data 1 (xD_D1).
xD_CD#	I	44	xD Card Detect (xD_CD).

5.9. GPO Pin

Table 9. GPO Pin

Symbol	Type	Pin No	Description
GPO	IO	38	General Purpose IO Pin (Used for Power Saving Feature).

5.10. Power and Ground

Table 10. Power and Ground

Symbol	Type	Pin No	Description
DVDD33	P	6, 31	Digital 3.3V Power Supply.
DVDD10	P	34	Digital 1.05V Power Supply.
EVDD10	P	18	LDO Regulator 1.05V Output.
Card_3V3	P	7	3.3V Power for All Cards.
VDD3318	P	26, 40	SD UHS Mode Power Supply.
CTRL10	P	47	LDO Regulator 1.05V Output.
AVDD33	P	1	Analog 3.3V Power Supply.
GND	P	25	Ground.
GND	P	49	Ground (Exposed Pad).

8.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 18. Absolute Maximum Ratings

Symbol	Description	Minimum	Maximum	Unit
AVDD33, CARD_3V3, DVDD33	Supply Voltage 3.3V	-0.3	3.6	V
DVDD10, EVDD10, CTRL10	Supply Voltage 1.05V	-0.3	1.32	V
3.3V DC Input 3.3V DC Output	Input Voltage Output Voltage	-0.3	3.6	V
1.05V DC Input 1.05V DC Output	Input Voltage Output Voltage	-0.3	1.32	V
N/A	Storage Temperature	-55	+125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

8.2. Recommended Operating Conditions

Table 19. Recommended Operating Conditions

Description	Pins	Minimum	Typical	Maximum	Unit
Supply Voltage VDD	AVDD33, CARD_3V3, DVDD33	3.14	3.3	3.46	V
	DVDD10, EVDD10, CTRL10	1.00	1.05	1.10	V
Ambient Operating Temperature T_A	-	0	-	70	°C
Maximum Junction Temperature	-	-	-	125	°C

Note: Refer to the most updated schematic circuit for correct configuration.

8.6. DC Characteristics

Table 23. DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
AVDD33/CARD_3V3/DVDD33	3.3V Supply Mean Voltage	-	3.14	3.3	3.46	V
DVDD10/EVDD10/CTRL10	1.05V Supply Mean Voltage	-	1.00	1.05	1.10	V
Voh	Minimum High Level Output Voltage	Ioh = -4mA	0.9*VDD33	-	VDD33	V
Vol	Maximum Low Level Output Voltage	Iol = 4mA	0	-	0.1*VDD33	V
Vih	Minimum High Level Input Voltage	-	2.0	-	-	V
Vil	Maximum Low Level Input Voltage	-	-	-	0.8	V
Iin	Input Current	Vin=VDD33 or GND	0	-	0.5	μA
Icc33	Maximum Operating Supply Current from 3.3V	At 1000Mbps with heavy network traffic and with Card Reader R/W operation	-	850	-	mA
Icc10	Maximum Operating Supply Current from 1.05V	At 1000Mbps with heavy network traffic and with Card Reader R/W operation	-	150	-	mA

Note 1: Refer to the latest schematic circuit for correct configuration.
Note 2: all Supply Mean Voltage power noise <±5% of Mean Voltage.

8.8.4. Auxiliary Signal Timing Parameters

Table 28. Auxiliary Signal Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{PERST}	Power Stable to PERSTB Inactive	100	-	ms
T_{REFCLK}	REFCLK Stable before PERSTB Inactive	100	-	μs
T_{PERST}	PERSTB Active Time	100	-	μs
$T_{PVRSMRT}$	PERSTB Rising Time Duration	50	-	ms
T_{PVR} *	Power Level Invalid to PWRGD Inactive	-	500	ns
T_{PVRG}	3.3Vaux Power On Time	1	-	ms

Note 1: T_{PER} means 100 ns (maximum) from the power rail going out of specification (exceeding the specified tolerances by more than 500 mV). Refer to PCI Local Bus Specification rev. 3.0 for further information. T_{PER} can be disregarded when implementation and timing of T_{PER} will not affect any L2/L3 functions.
Note 2: The ISOLATEB pin should follow the behavior of the 3.3V main power waveform.

Figure 17. Auxiliary Signal Timing

6. Power Sequence

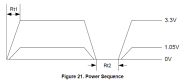
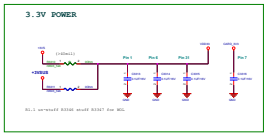


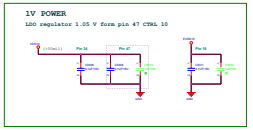
Figure 21. Power Sequence

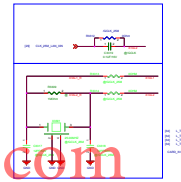
Table 1. Power Sequence Parameter

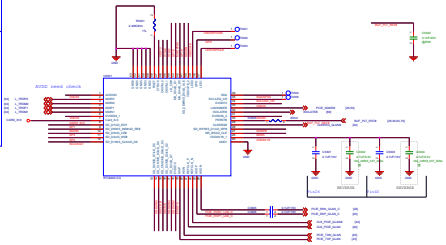
Symbol	Description	Min	Typical	Max	Units
R11	3.3V Rise Time	1	-	100	ms
R12	3.3V Off Time	50	-	-	ms

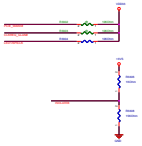
Note 1: The RTL8402 does not support Hot 3.3V rising. The 3.3V rise time must be controlled over 1ms.
Note 2: If there is any action that involves consecutive ON/OFF toggling of the LDO regulator source (3.3V) and output (1.05V) reach Off, and the time period between the consecutive ON/OFF toggling action must be longer than 10ms.

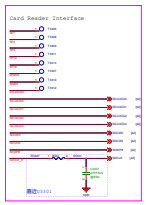


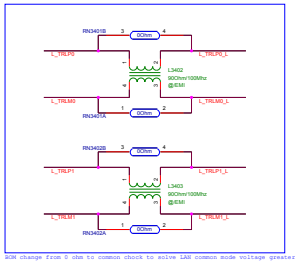


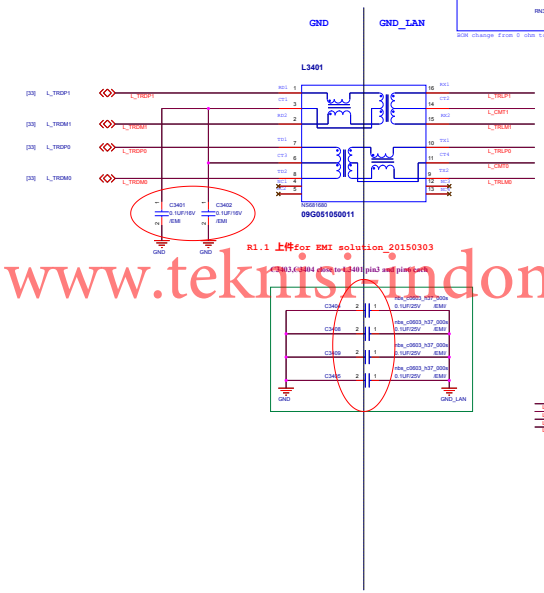


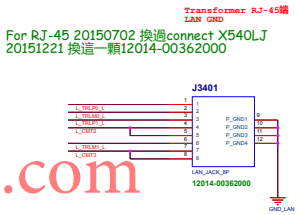


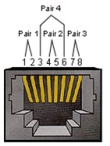




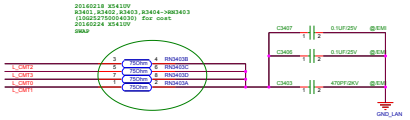


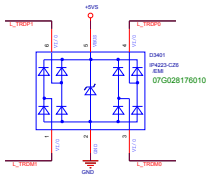


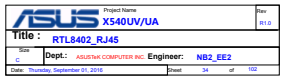




RJ45連接腳位	傳輸訊號
1	Tx +
2	Tx -
3	Rx +
4	No Singal
5	No Singal
6	Rx -
7	No Singal
8	No Singal

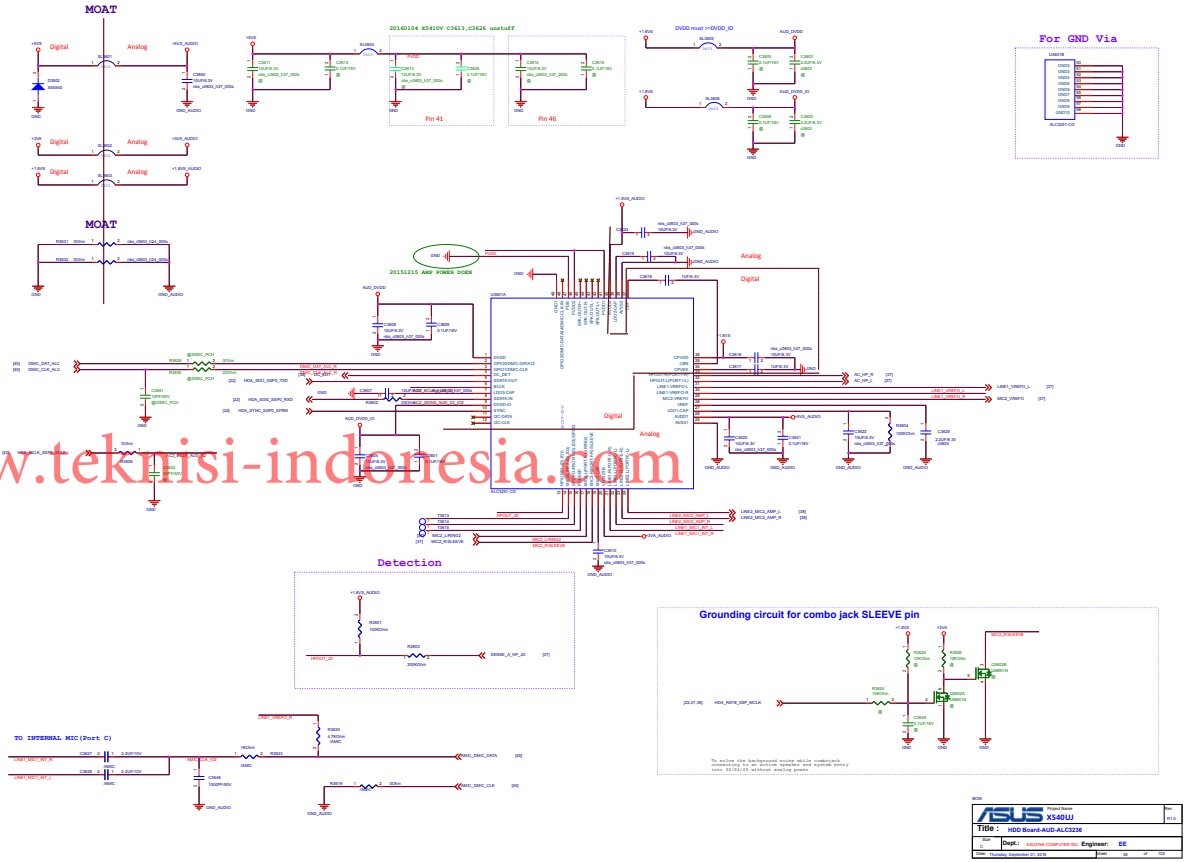






Schematic Page List Hide

- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
- 032_RST_Reset Circuit
- 033_RTL8402 (LAN+CR)
- 034_RTL8402_RJ45
- 035_****
- 036_AUD-ALC3251
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTOR
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor



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- 027_CPU_PCH_POEWR,GND
- 028_PCH-SPI ROM,OTH,DEBUG
- 029. Silego_Green_CLK_Gen___
- 030_IT8995E-128/CX
- 031_KBC_KB,TP,KB-light
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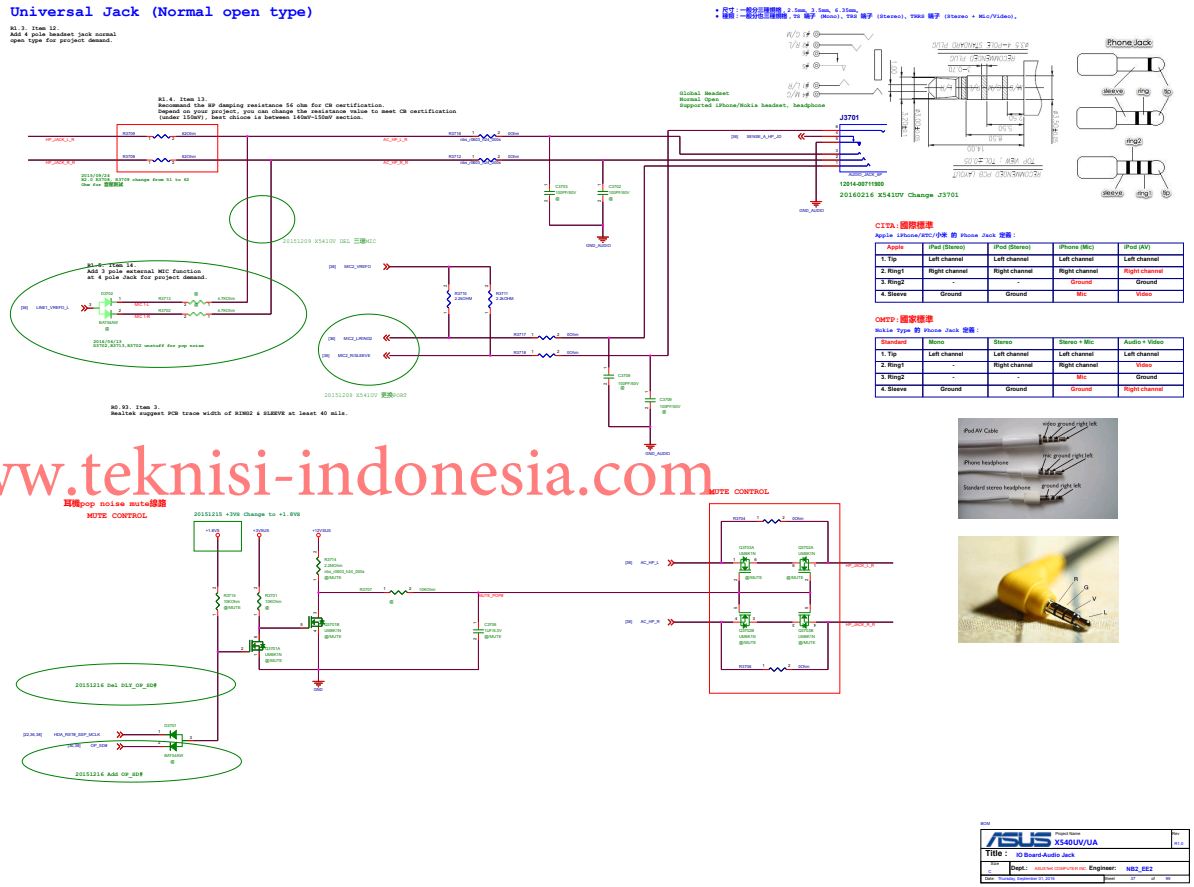
- 037_AUD-HEADPHONE JACK
- 038_AMP_Speaker
- 039_
- 040_
- 041_****
- 042_CARD READER CONNECTOR
- 043_****
- 044_
- 045_eDP_LVDS
- 046_
- 047_eDP to VGA & CRT D-SUB
- 048_HDMI-type A
- 049_
- 050_FAN_Thermal Sensor



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028_PCH-SPI ROM,OTH,DEBUG
029. Silego_Green_CLK_Gen___
030_IT8995E-128/CX
031_KBC_KB,TP,KB-light
032_RST_Reset Circuit
033_RTL8402 (LAN+CR)
034_RTL8402_RJ45
035_****
036_AUD-ALC3251
037_AUD-HEADPHONE JACK
038_AMP_Speaker
039_
040_
041_****
042_CARD READER CONNECTOR
043_****
044_
045_eDP_LVDS
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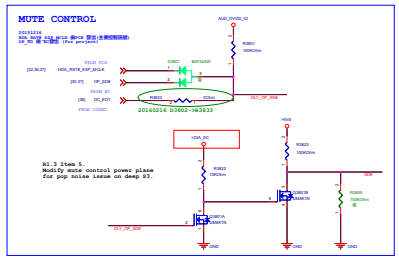
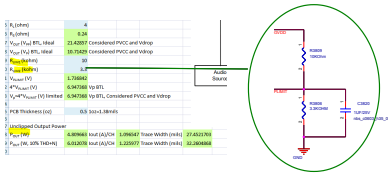
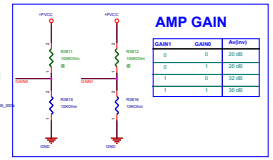
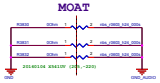
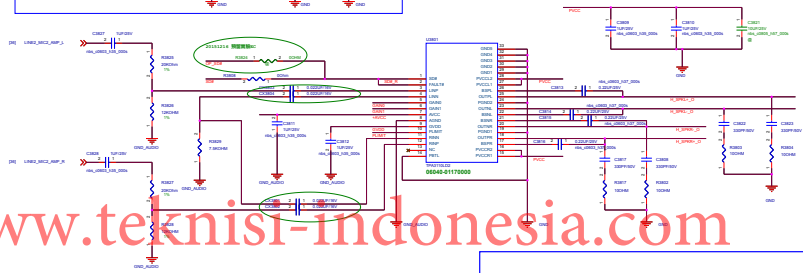
047_eDP to VGA & CRT D-SUB
048_HDMI-type A
049_
050_FAN_Thermal Sensor

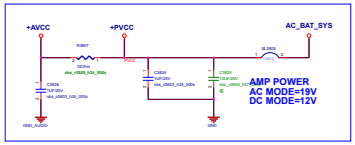


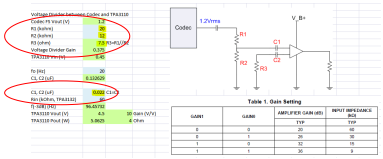


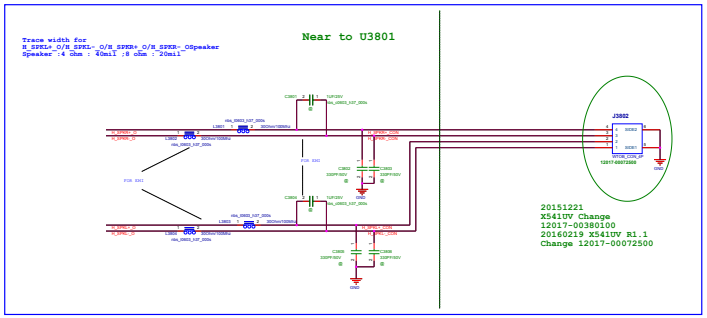












12023-00013700

SD CARD PIN DESIGN

Pin No.	Name	Description
1#	CD/DAT3	Card detect/Data I/O
2#	CMD	Command
3#	VSS1	Ground
4#	VDD	Power
5#	CLK	Clock
6#	VSS2	Ground
7#	DAT0	Data I/O
8#	DAT1	Data I/O
9#	DAT2	Data I/O

10-CARD DETECT PIN
11-WRITE PROTECT PIN
GROUND(SHELL)--COMMON PIN

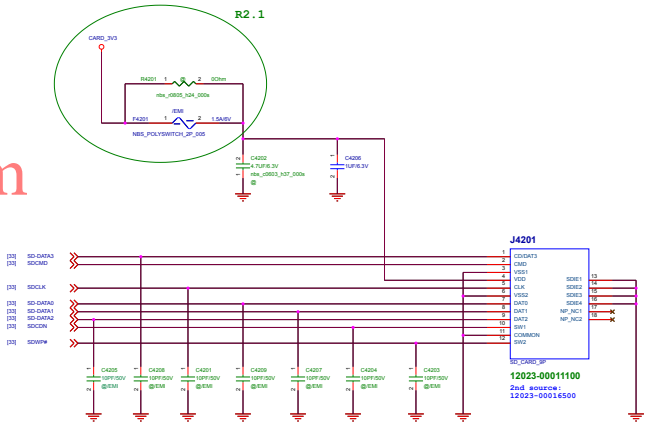
RTL8402-CG		CARD_READER_CONNECTOR_SIDE		
SD_WP	LOCK:H UNLOCK:L	PIN 11	WRITE PROTECT PIN	LOCK:H UNLOCK:L
SD_CD#	DETECT:L UNDETECT:FLOATING	PIN 10	CARD DETECT PIN	DETECT:L UNDETECT:FLOATING

12023-00015500

Without card: CD/GND 狀態為開路 WP/CD狀態 開路
Insert card (unlock):CD/GND 短路 WP/CD開路
Insert card (lock):CD/GND 短路 WP/CD開路

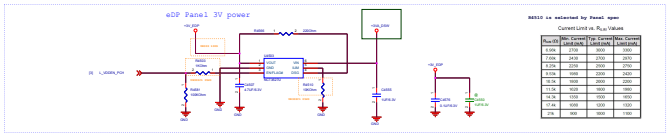
R1.1
Removed Q0501 and RN0501 for J0501 SDWP/SDCD signal reverse circuit

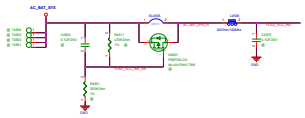
R2.1
移除SL0501改上R0501

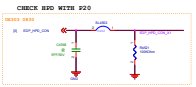


ASUS X540UV/UA
Title : CARD READER CONNECTOR
Dept.: Engineer: NB2_EE2

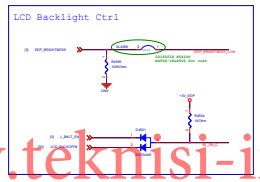
eDP (LVDS) Panel

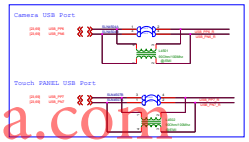


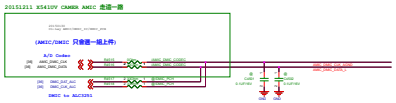


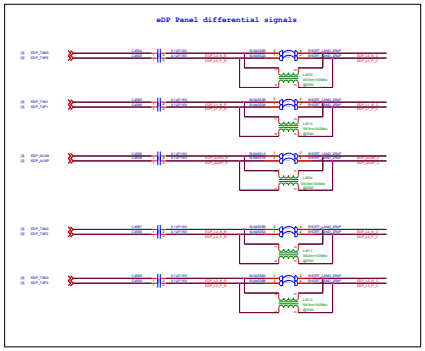


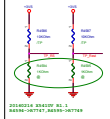
teknisi-indonesia

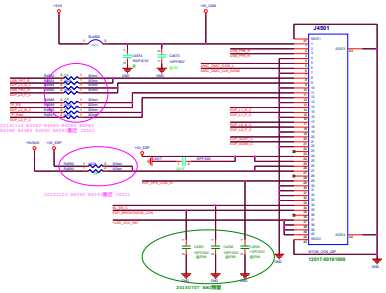


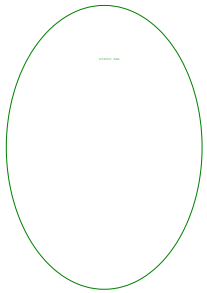






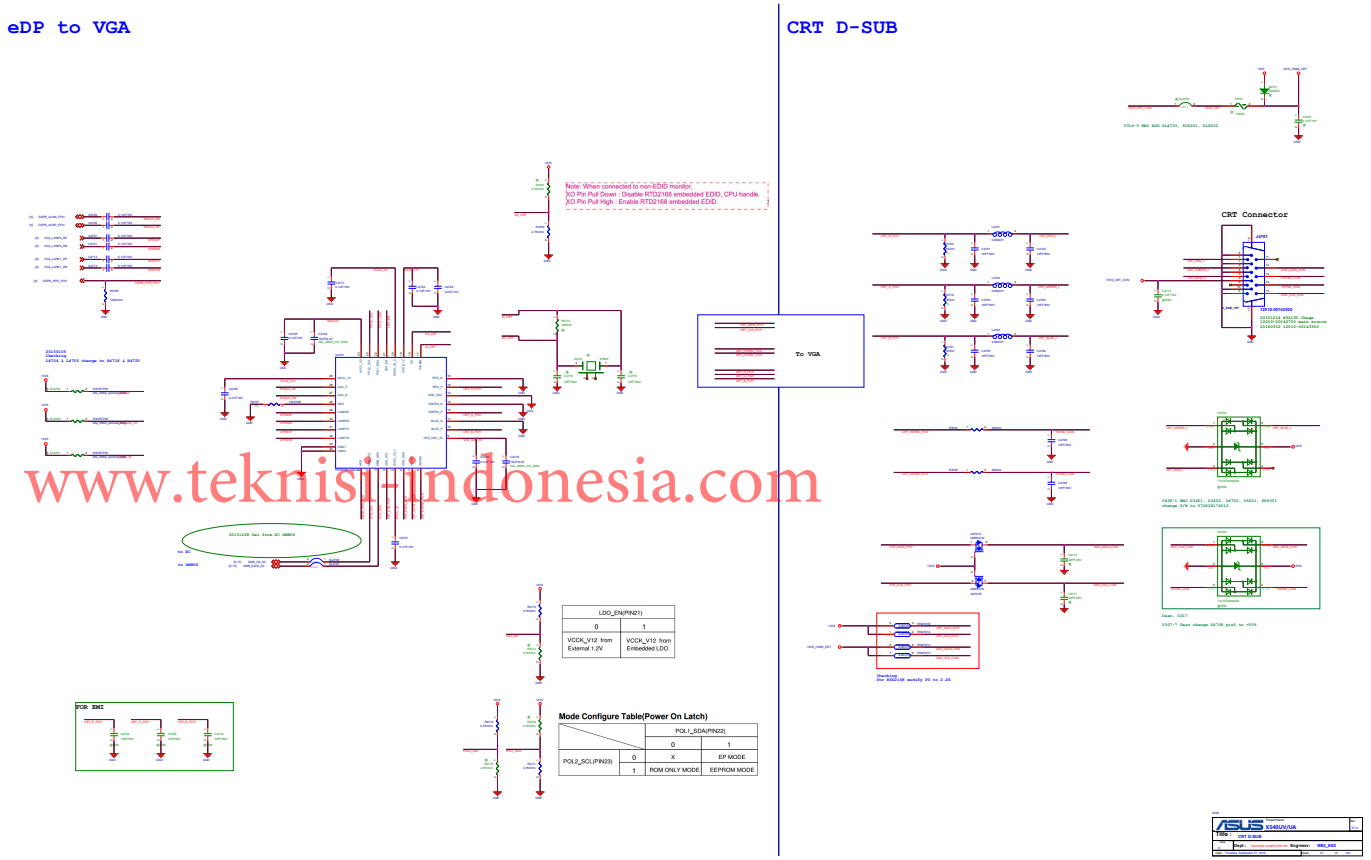




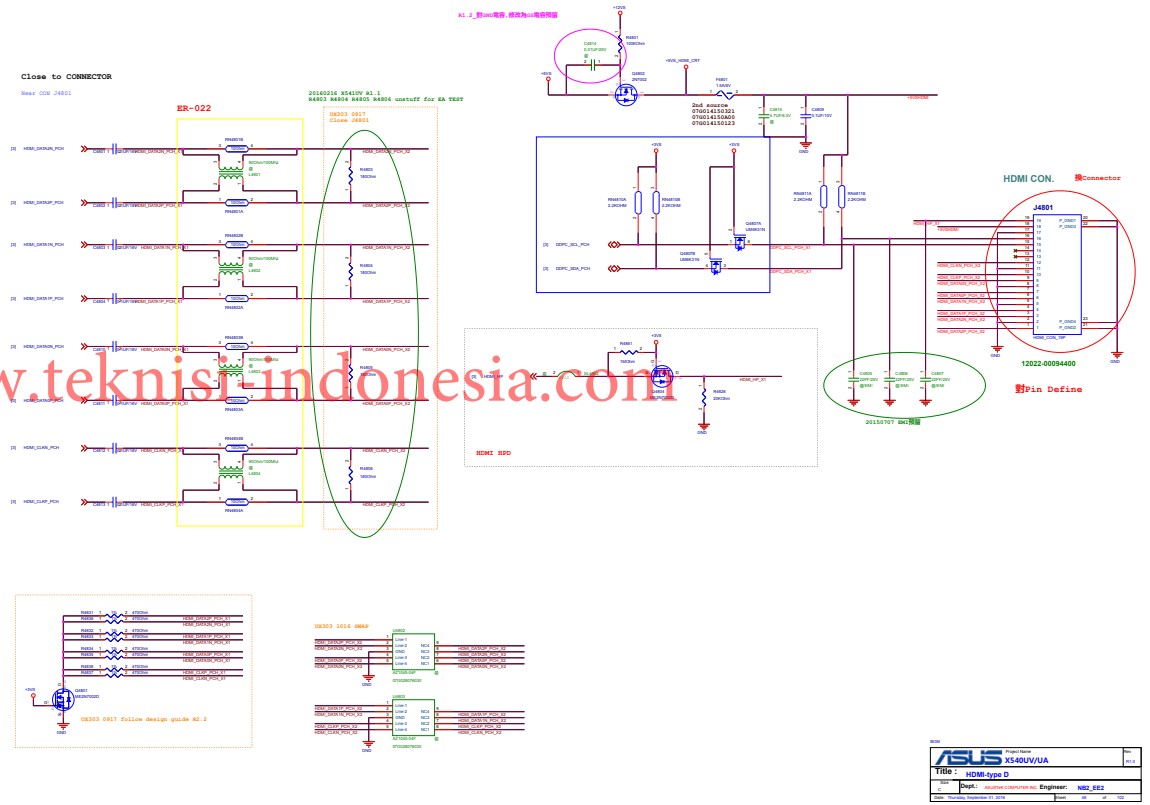


BOM

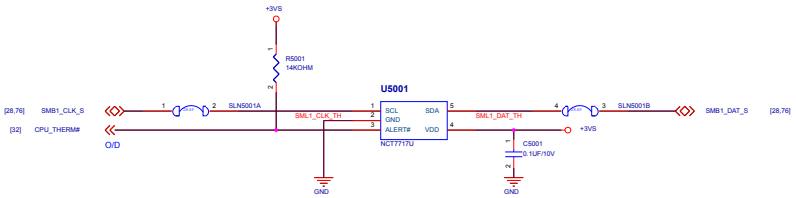
ASUS	Project Name: X540UV/UA	Rev: R1.0
Title :	LCD Panel_CMOS_DMIC	
Size: D	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet 45 of 102	



HDMI type-A



CPU Thermal Sensor



5.3 Address Setting

NCT7717U I2C/SMBus address is 1001000xb (x is R/W bit).

5.6 ALERT# point hardware power-on setting (TBD)

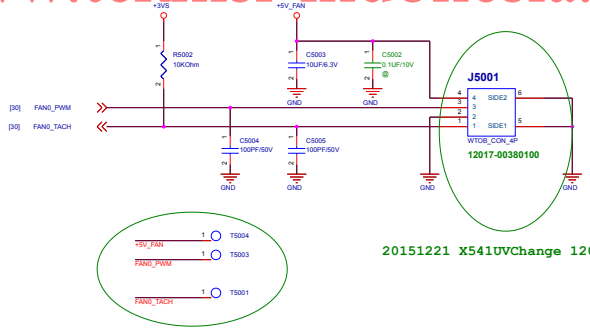
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin :

PULL-UP RESISTOR		TEMPERATURE (℃)
ALERT	2KΩ	75
	7.5KΩ	90
	10.5KΩ	100
	14KΩ	105
	18.7KΩ	110

Route CPU_THRM_DA , CPU_THRM_DC and on the same layer

----------OTHER SIGNALS
10 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
==========GND
10 mils
----------OTHER SIGNALS
Avoid FSB,Power

DC FAN Control



20151221 X541UVChange 12017-00380100

請將測點至於TOP面
R2.0 新增_Tim_20150820

<Variant Name>

ASUSTeK COMPUTER INC. NB3

Title : 50_FAN_Thermal Sensor

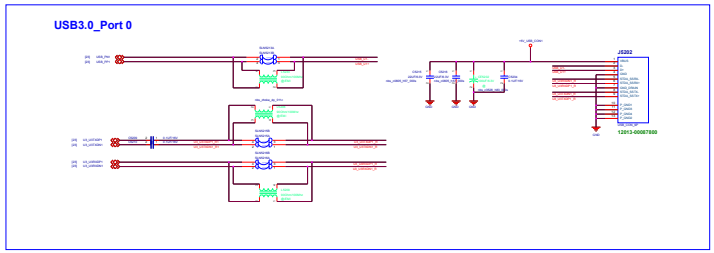
Engineer: NB2_EE2

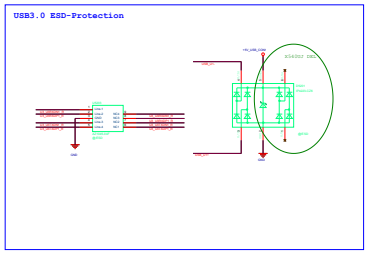
Size: B | Project Name: X540UV/UA | Rev: R1.0

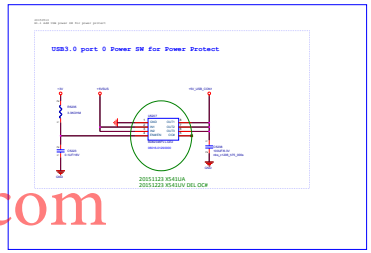
Date: Thursday, September 01, 2016 | Sheet 50 of 99

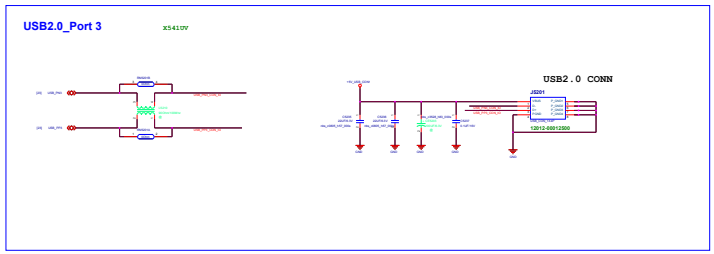
Schematic Page List Hide

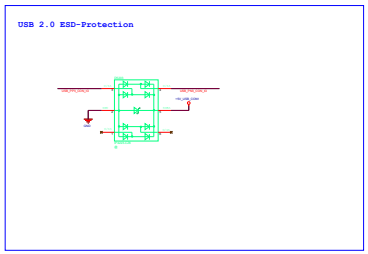
044_
045_eDP_LVDS
046_
047_eDP to VGA & CRT D-SUB
048_HDMI-type A
049_
050_FAN_Thermal Sensor
051_
052_USB 3.0 + 2.0 CONN.
053_MINICARD(WLAN)
054_
055_USB 3.1 MB Type-C
056_***
057_DSG_Discharge
058_PRO_Protect
059_Power & WIFI & CAP LED&LID
060_DC_DC & BAT IN
061_****
062_
063_
064_
065_ME_Conn & Skew Hole
066_
067_***
068_B to B connector_HDD_ODD





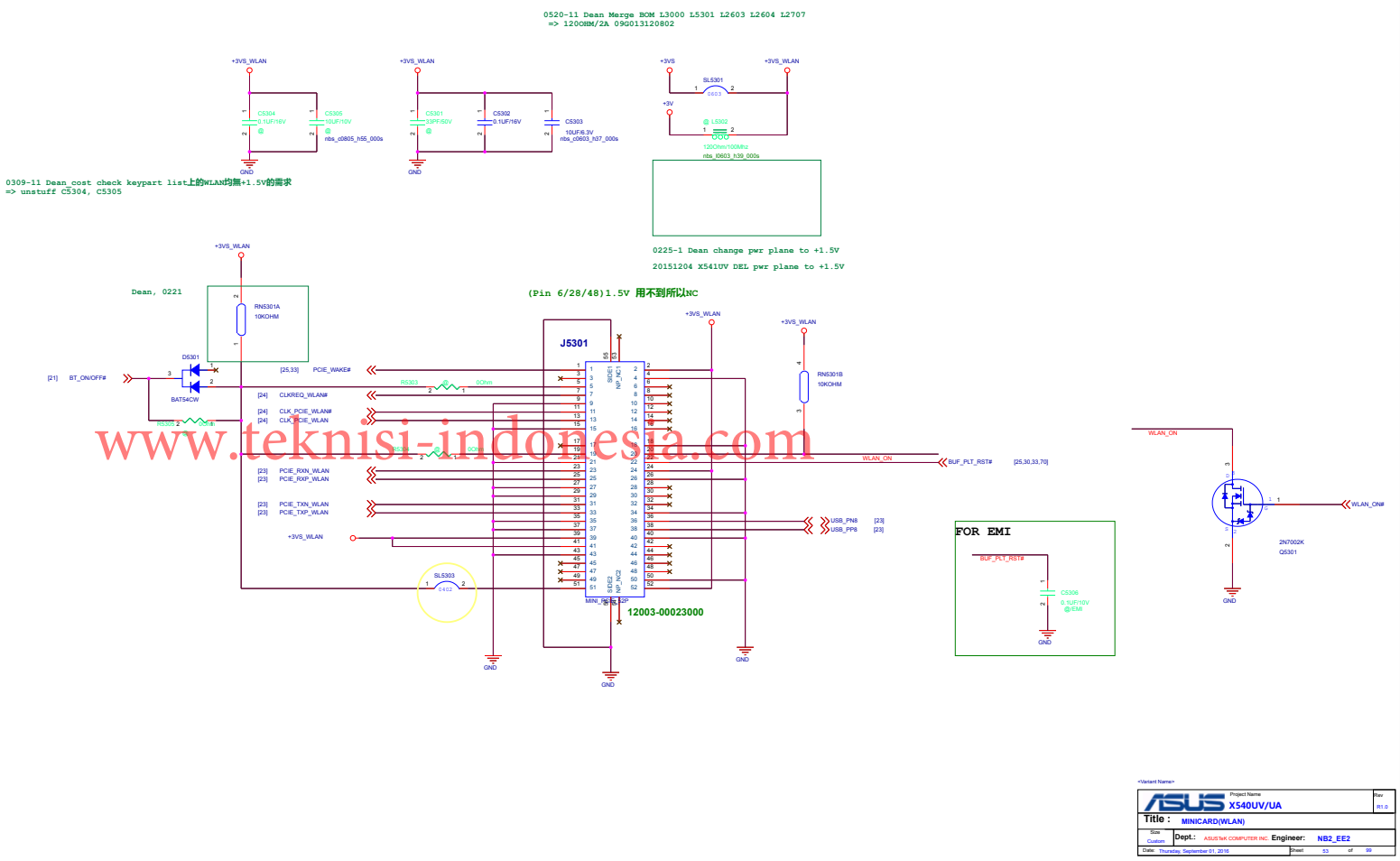


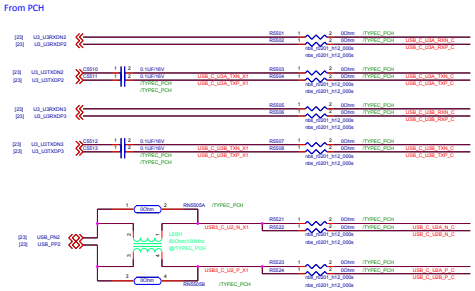


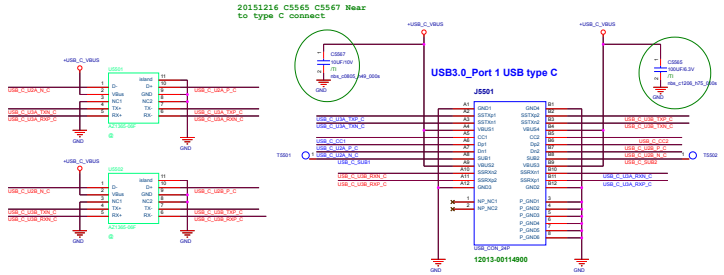


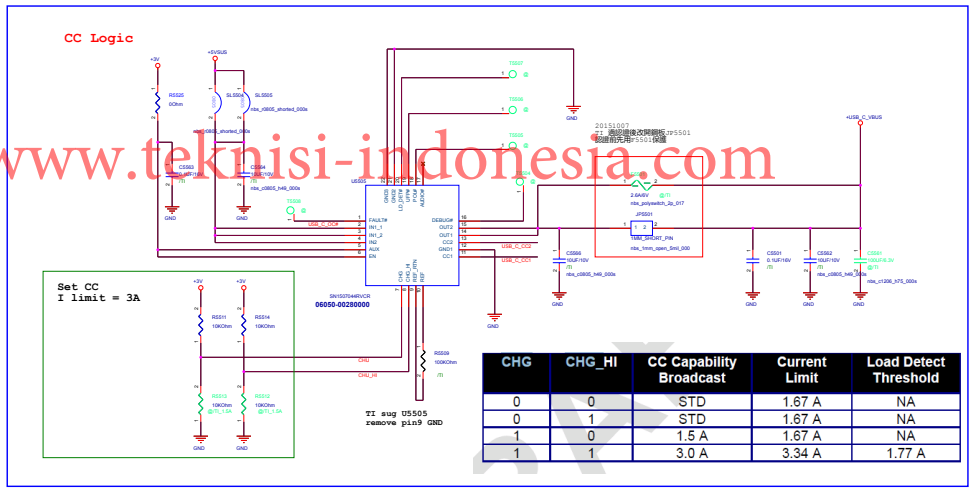
Schematic Page List Hide

044_
045_eDP_LVDS
046_
047_eDP to VGA & CRT D-SUB
048_HDMI-type A
049_
050_FAN_Thermal Sensor
051_
052_USB 3.0 + 2.0 CONN.
053_MINICARD(WLAN)
054_
055_USB 3.1 MB Type-C
056_***
057_DSG_Discharge
058_PRO_Protect
059_Power & WIFI & CAP LED&LID
060_DC_DC & BAT IN
061_****
062_
063_
064_
065_ME_Conn & Skew Hole
066_
067_***
068_B to B connector_HDD_ODD









CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A

ASUS	Project Name: X540UV/UA	Rev: R1.0
Title : USB 3.1 MB Type-C		
Size: C	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet: 55 of 102	

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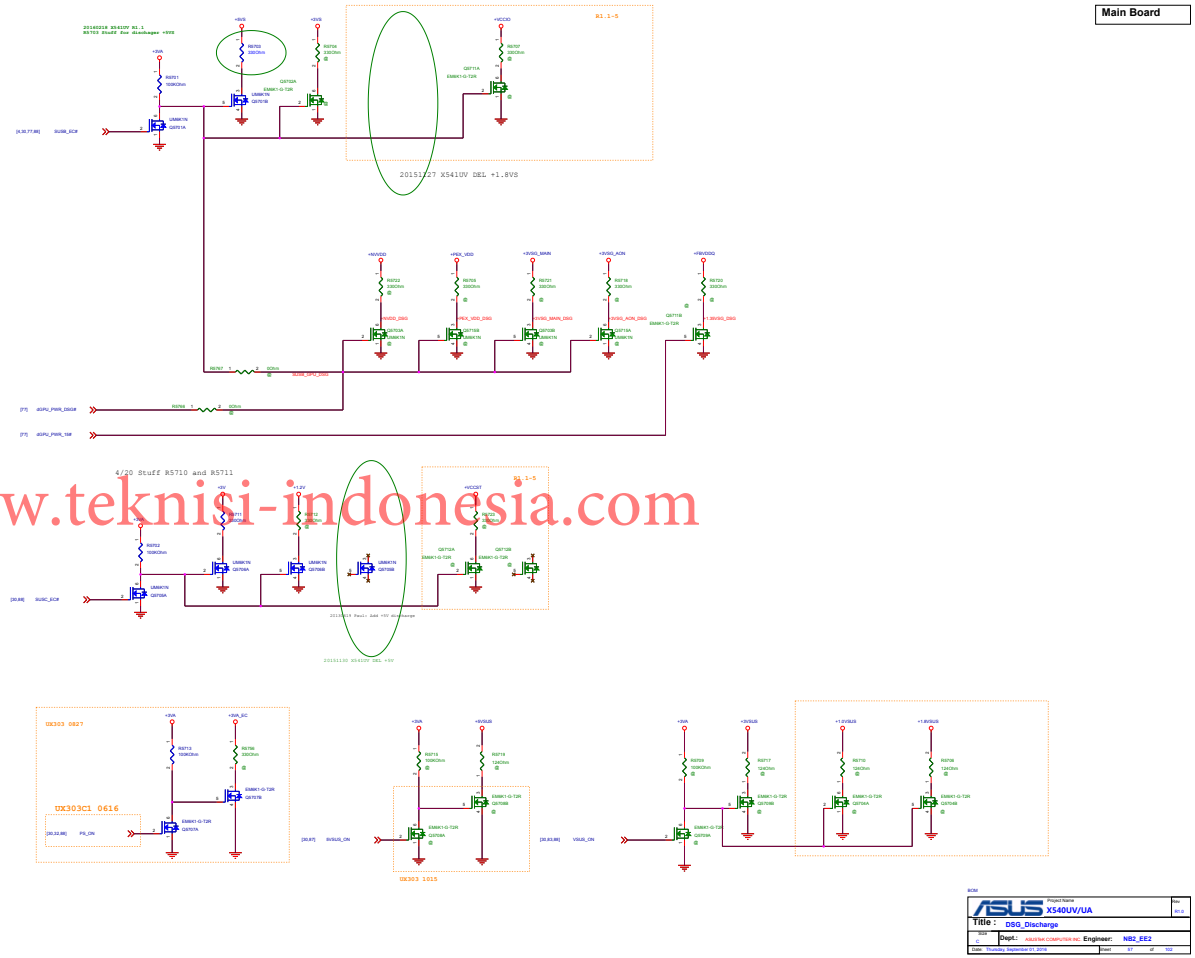
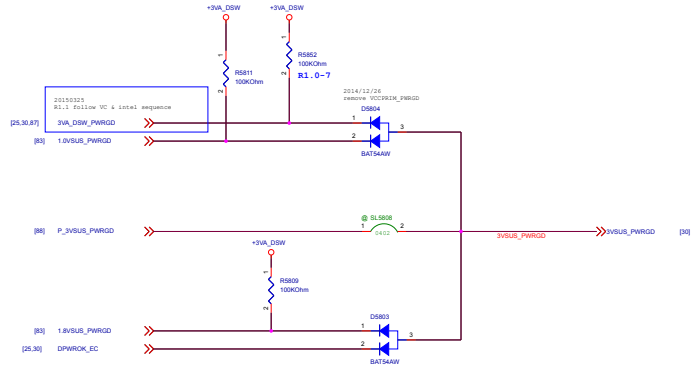
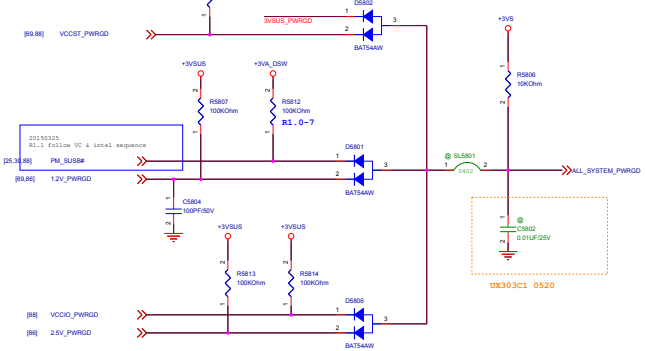
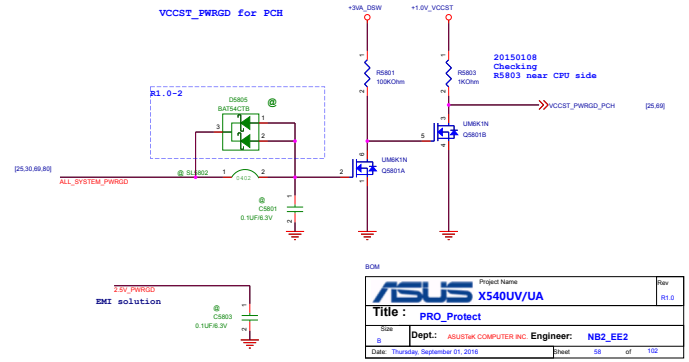
044_
045_eDP_LVDS
046_
047_eDP to VGA & CRT D-SUB
048_HDMI-type A
049_
050_FAN_Thermal Sensor
051_
052_USB 3.0 + 2.0 CONN.
053_MINICARD(WLAN)
054_
055_USB 3.1 MB Type-C
056_***
057_DSG_Discharge
058_PRO_Protect
059_Power & WIFI & CAP LED&LID
060_DC_DC & BAT IN
061_****
062_
063_
064_
065_ME_Conn & Skew Hole
066_
067_***
068_B to B connector_HDD_ODD

Main Board

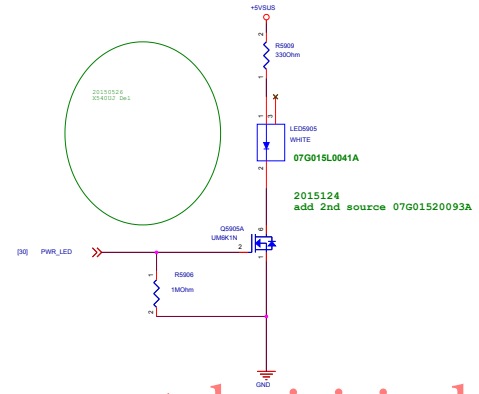






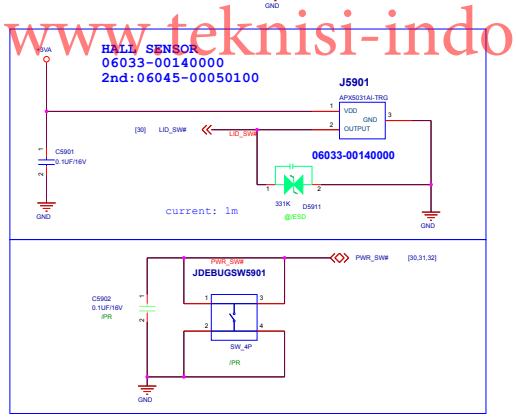


POWER LED



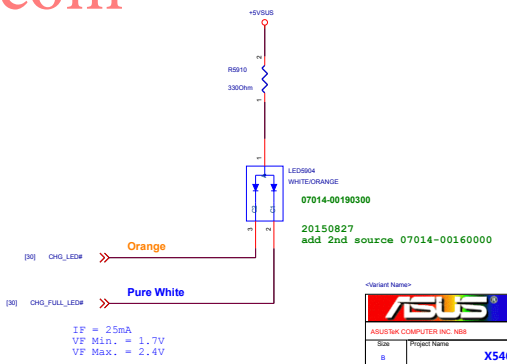
WIRELESS/ BT LED

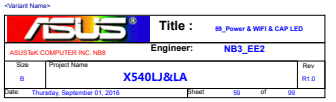
CAP Lock LED

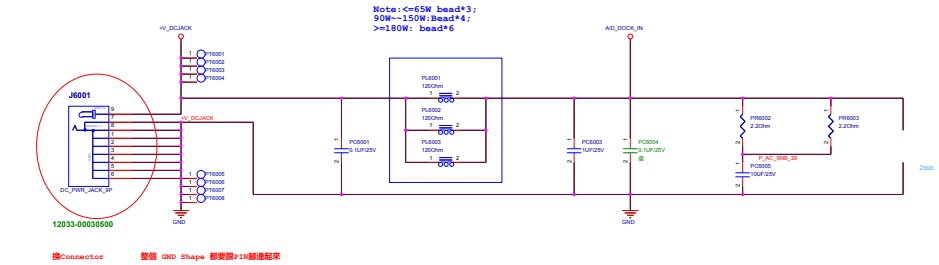


LED indicator

Charger LED

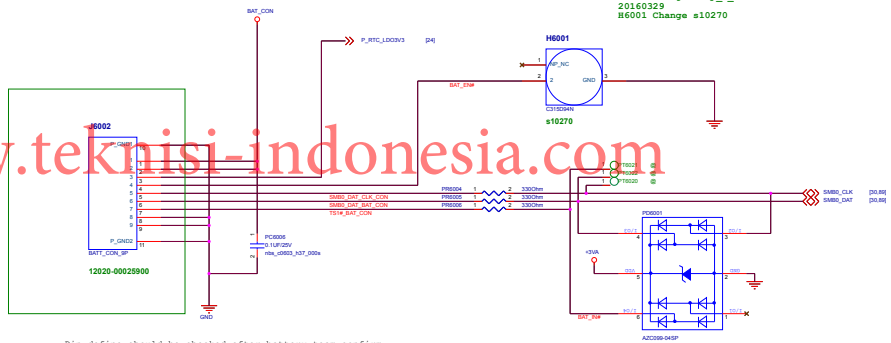






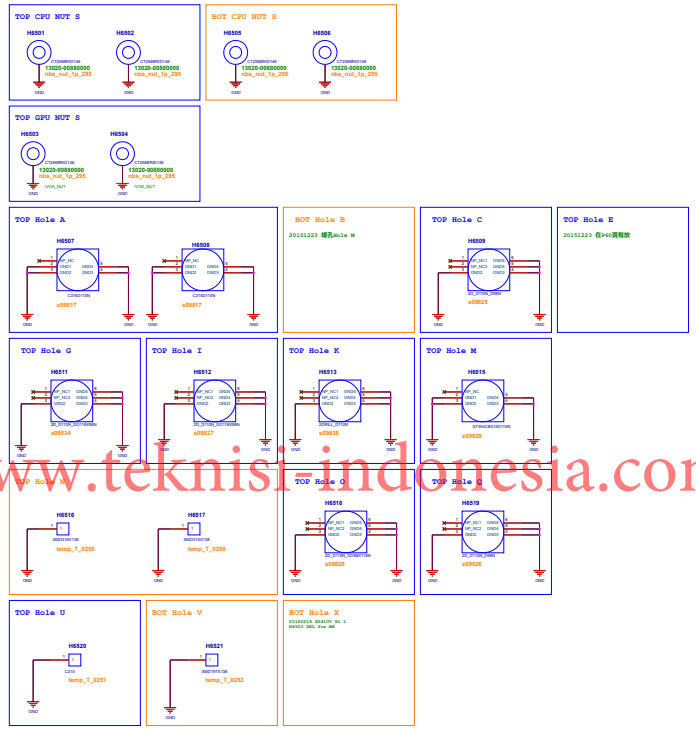
Battery Connector

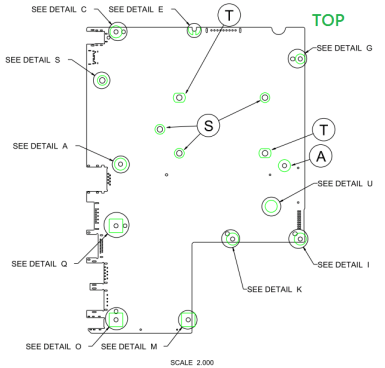
20150706
H6001為一顆螺絲接通 BAT_EN# 和 GND,電池才開始送電
20160216
H6001 Change temp_P_0390
20160329
H6001 Change s10270

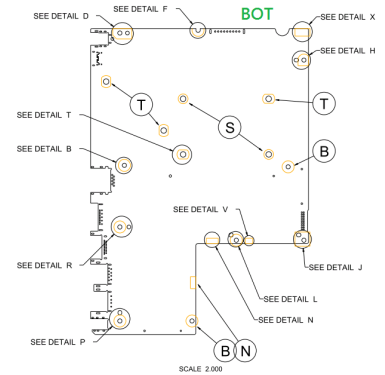


Pin define should be checked after battery team confirm

Pin Seq.	Name	Description	Remark
1	P+	Battery pack positive terminal	Output voltage
2	P+	Battery pack positive terminal	Output voltage
3	LDO 3.3V		
4	EN#	External charge & discharge Mosfet control pin.	SYSTEM Connection to GND for charge & discharge
5	SMBC	Serial clock input	SMBC
6	SMBD	Serial data input	SMBD
7	BAT_IN#	EC detect battery_in pin	PACK inside 0 Ω connect to GND
8	P-	Battery pack negative terminal.	GND
9	P-	Battery pack negative terminal.	GND

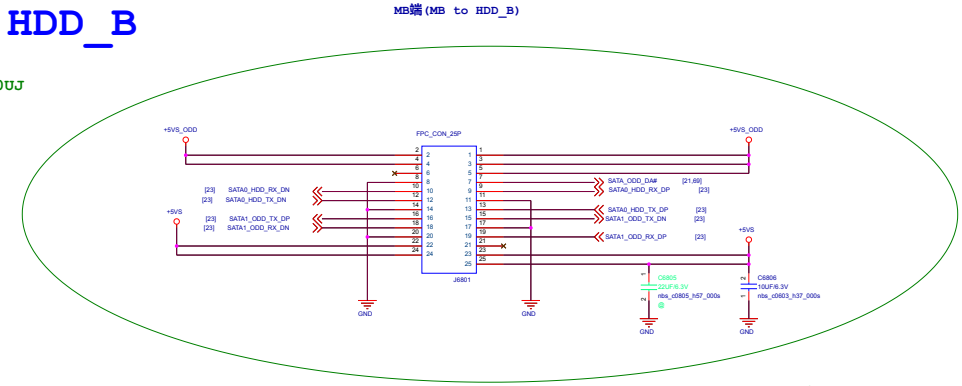




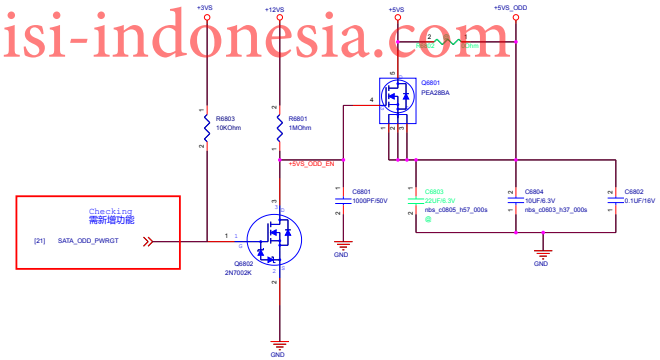


MB to HDD_B

20150520 X540UJ



20160630 X541UAK/UVK follow X441 change FPC Connector



BOM

ASUS	Project Name: X540UV/UA	Rev: R1.0
Title : B TO B CONNECTOR		
Size: B	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet 68 of 99	

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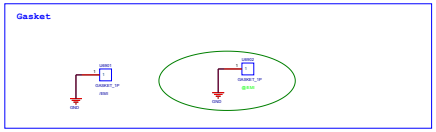
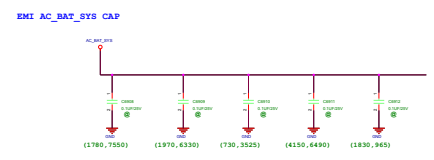
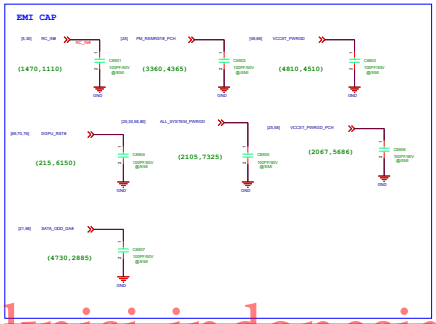
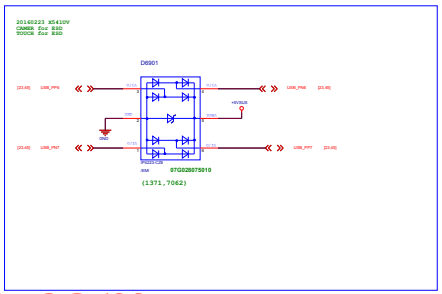
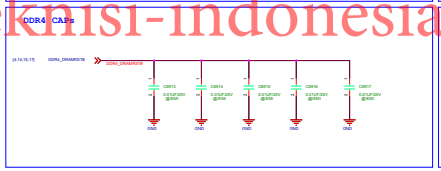
- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DDR3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

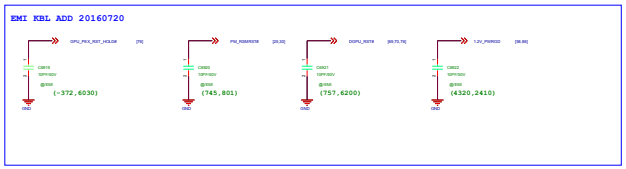












BOM

ASUS Project Name: X540UV/UA

Title : EMI

Dept.: Engineer: NB2_EE2

Date: Thursday, September 01, 2016

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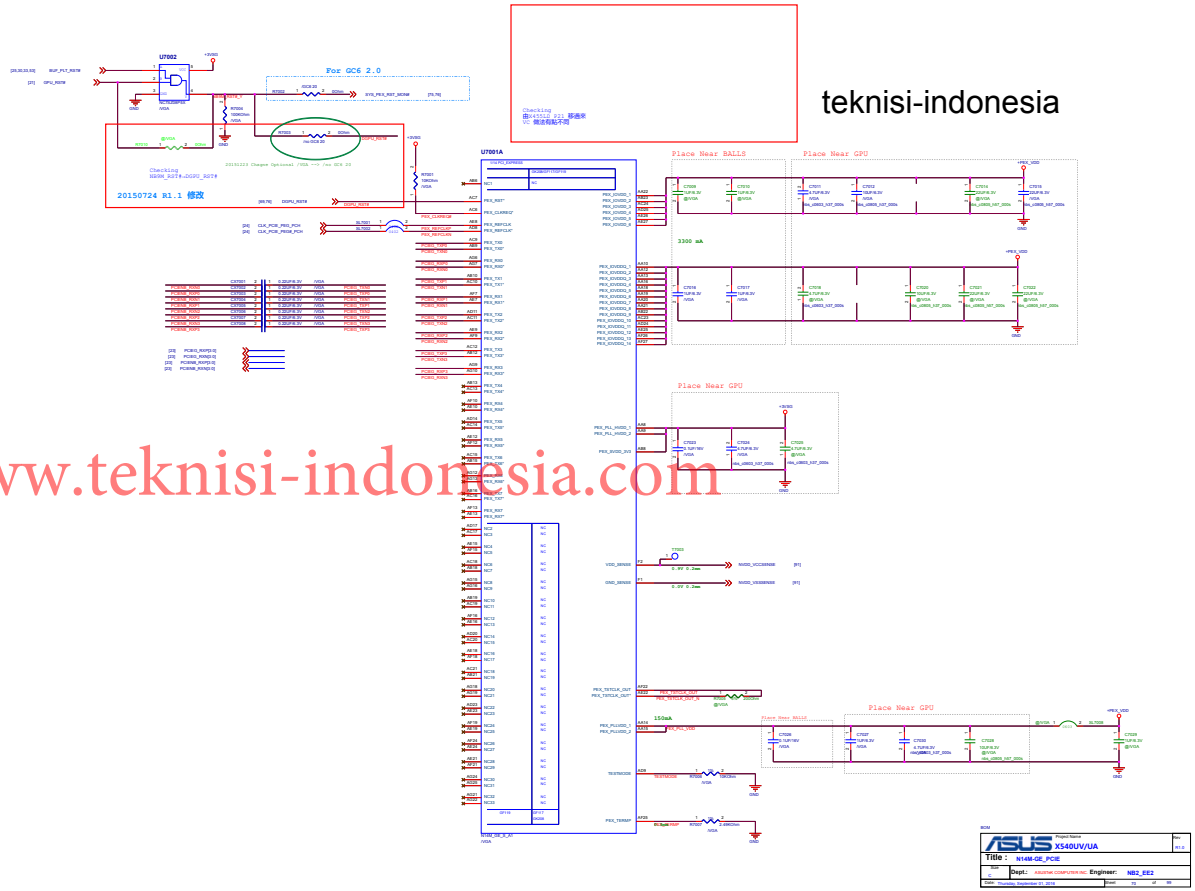
- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DDR3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS



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- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DDR3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

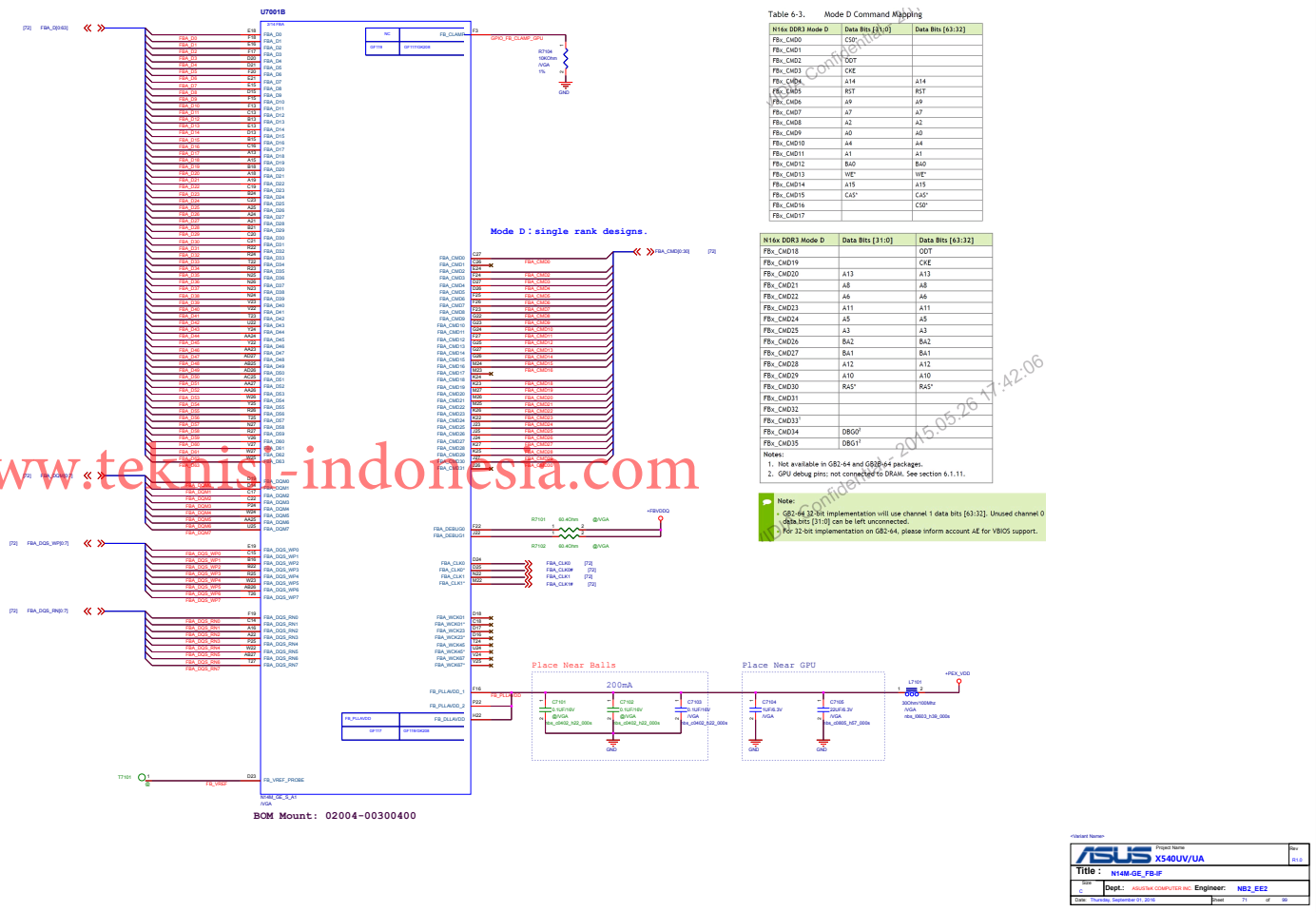

Table 6-3. Mode D Command Mapping

N16x DDR3 Mode D	Data Bits [31:0]	Data Bits [63:32]
FBx_CMD0	CS0*	
FBx_CMD1		
FBx_CMD2	ODT	
FBx_CMD3	CKE	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE*	WE*
FBx_CMD14	A15	A15
FBx_CMD15	CAS*	CAS*
FBx_CMD16		CS0*
FBx_CMD17		
FBx_CMD18		ODT
FBx_CMD19		CKE
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS*	RAS*
FBx_CMD31		
FBx_CMD32		
FBx_CMD33[1]		
FBx_CMD34	DBG0[2]	
FBx_CMD35	DBG1[2]	

Notes:
1. Not available in GB2-64 and GB2B-64 packages.
2. GPU debug pins; not connected to DRAM. See section 6.1.11.

Note:
- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel 0 data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.

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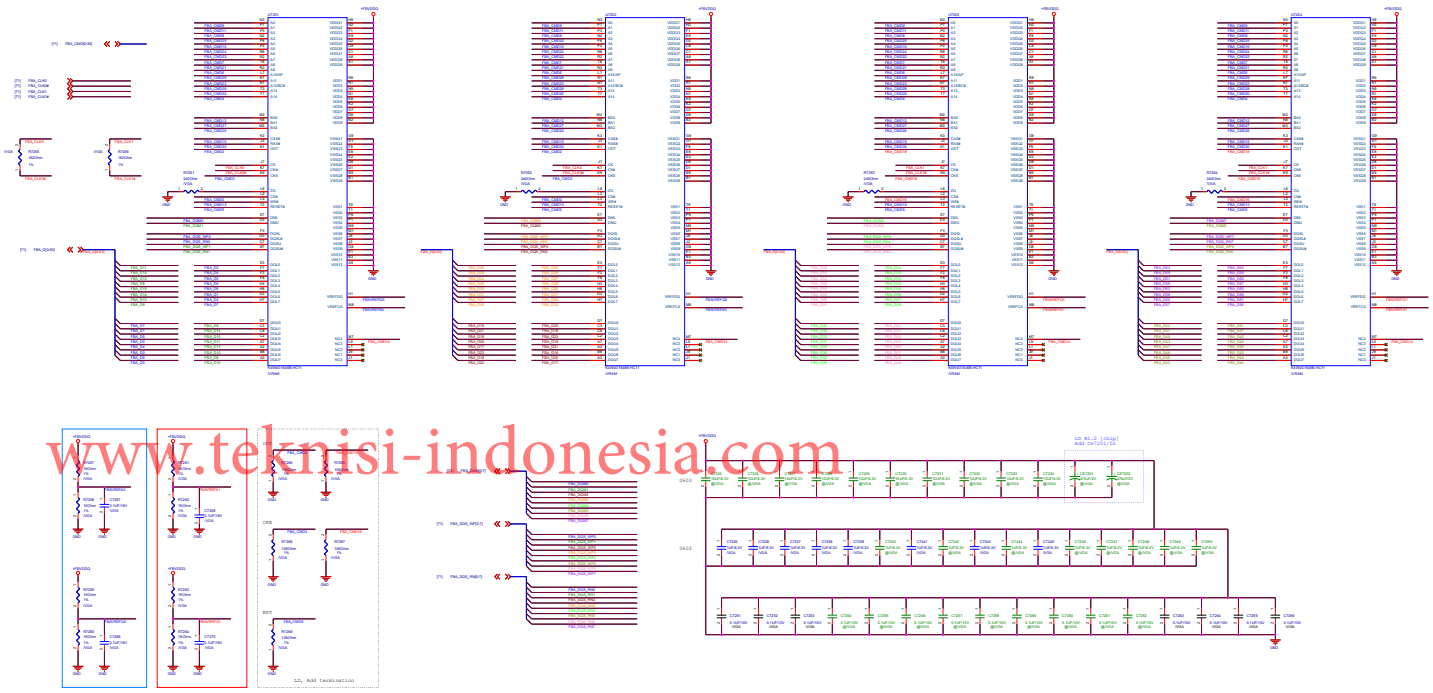
- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPL AY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWE R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

Global Search | 081 | 080 | 077 | 076 | 075 | 074 | 073 | 072 | 071 | 070 | 069

Toggle FullScreen | Pre Page | Next Page | MoveTo



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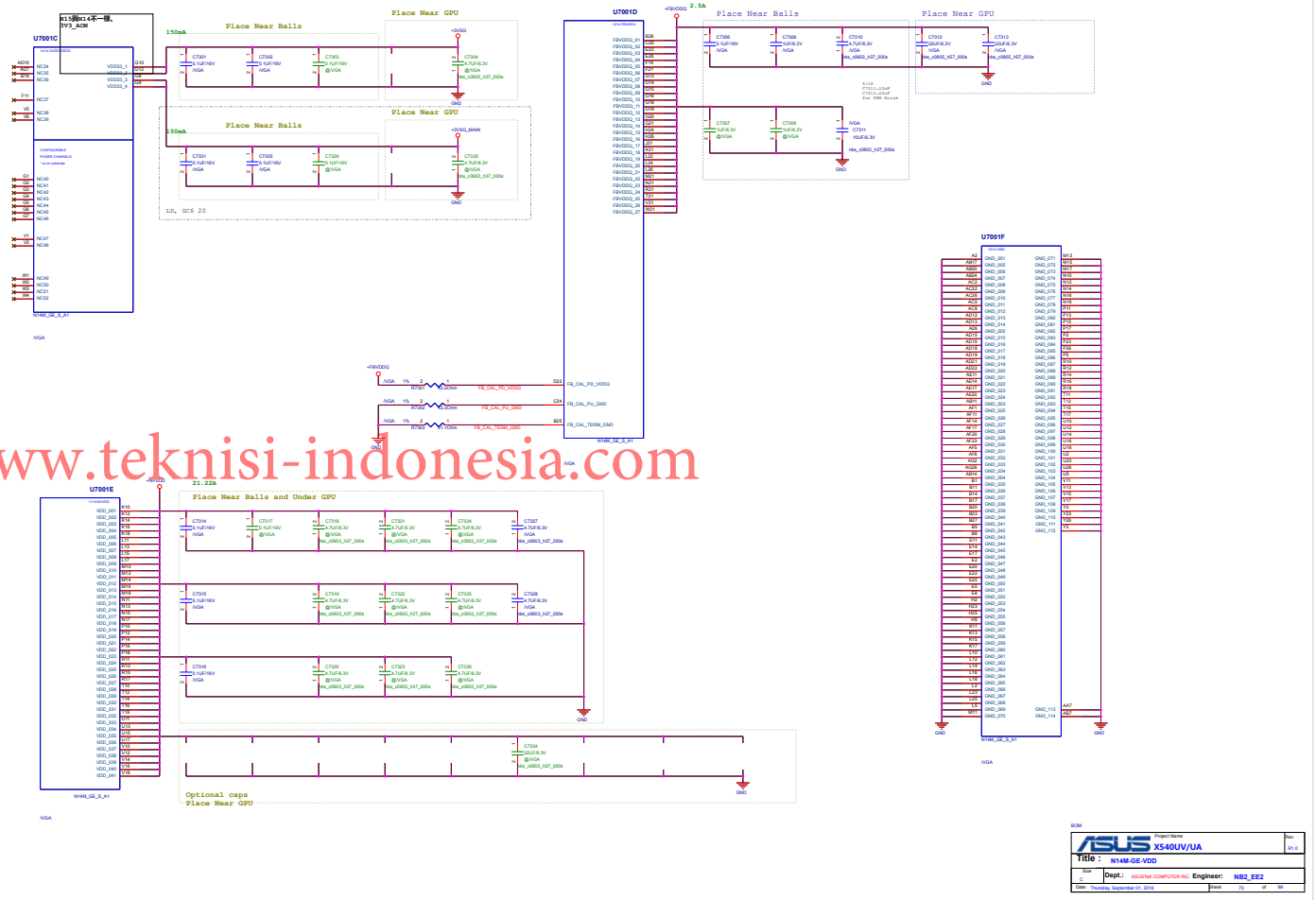
- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DD R3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPL AY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWE R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS



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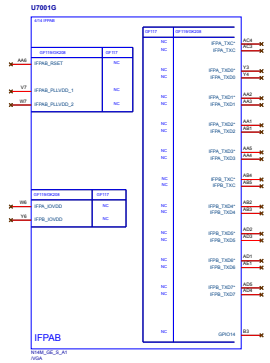
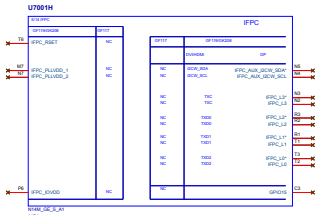
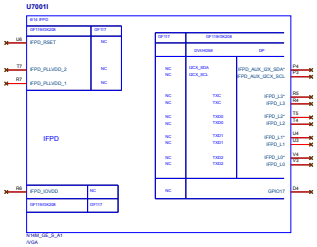
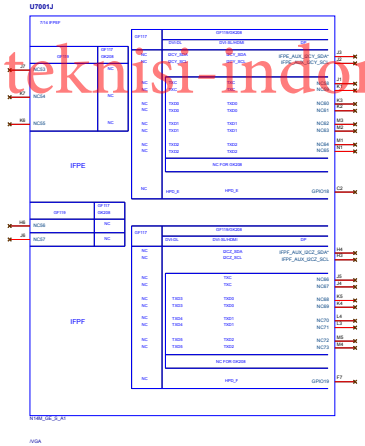
- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DDR3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS

LVDS

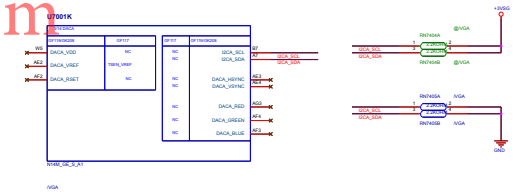








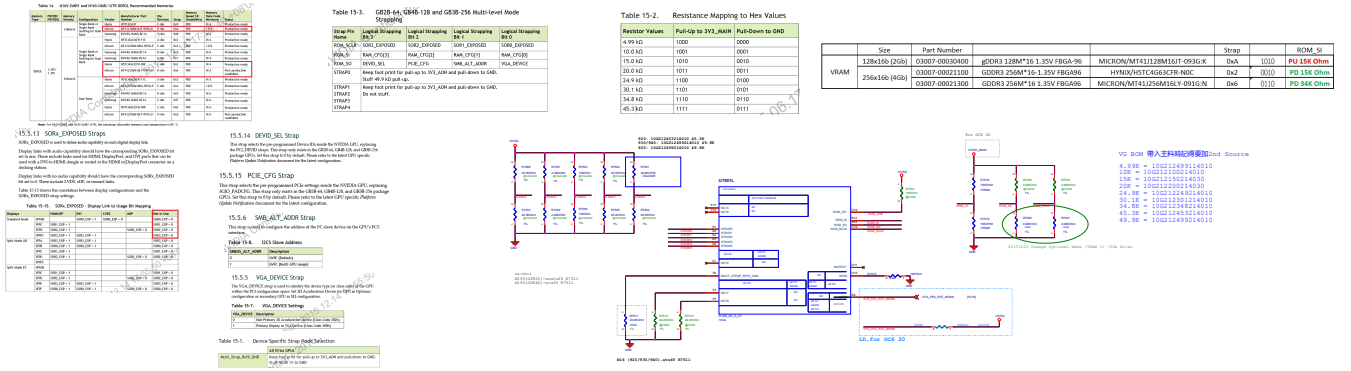
CRT



ASUS	Project Name: X540UV/UA	Rev: 2.0
Title :	N14M-GE_DISPLAY	
Size: A	Dept.: ASUSTeK COMPUTER INC.	Engineer: NB2_EE2
Date: Thursday, September 01, 2016	Sheet 74 of 99	

Schematic Page List Hide

- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DDR3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS



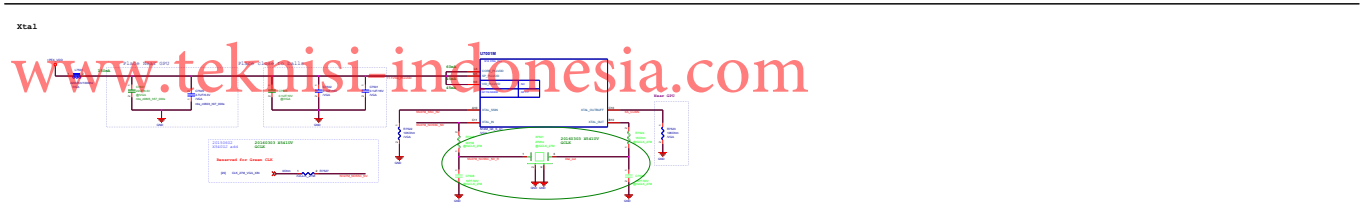
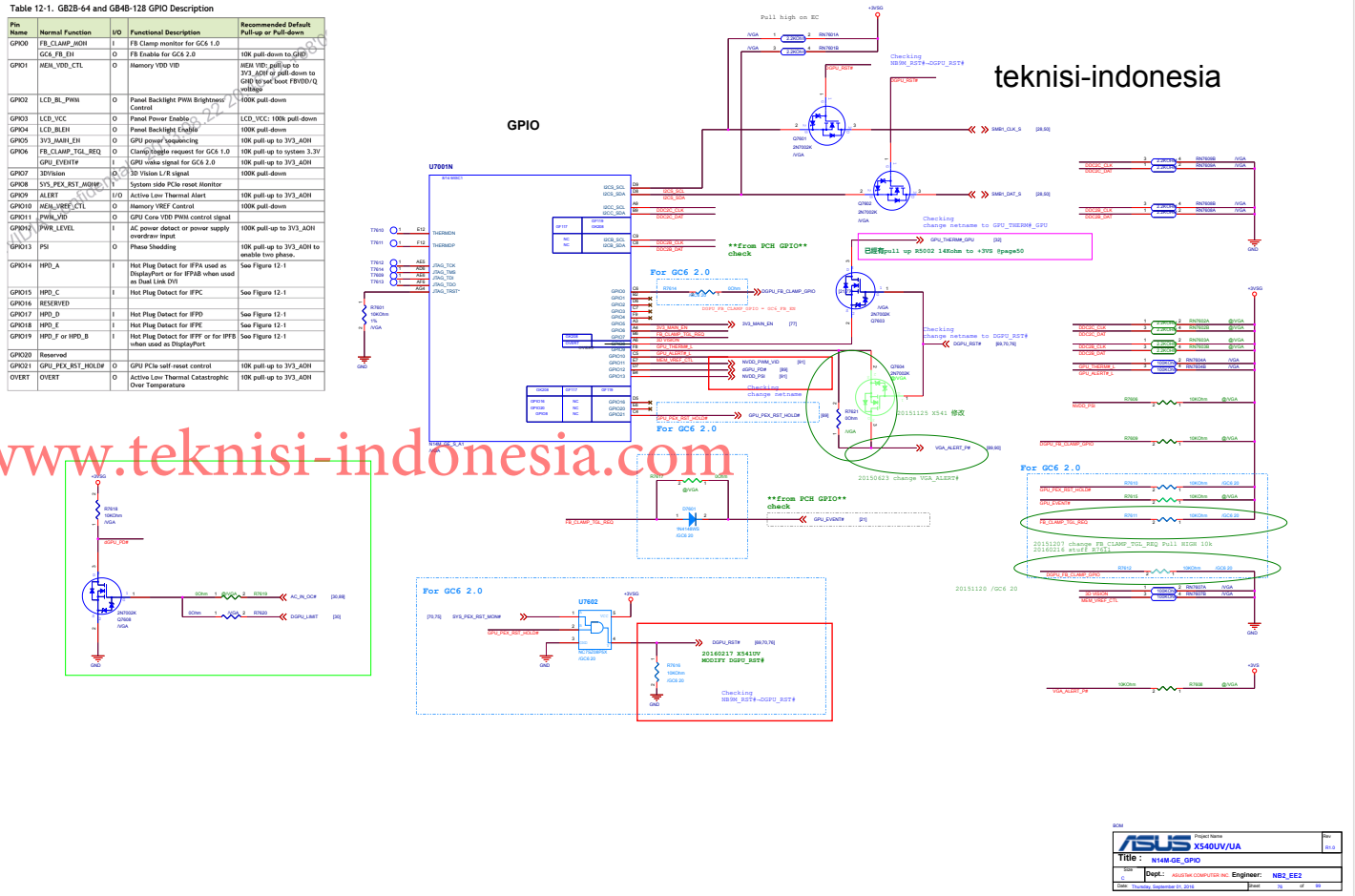


Table 12-1. GB2B-64 and GB4B-128 GPIO Description

Pin Name	Normal Function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	FB_CLAMP_MOH	I	FB Clamp monitor for GC6 1.0	
	GC6_FB_EH	O	FB Enable for GC6 2.0	10K pull-down to GND
GPIO1	MEM_VDD_CTL	O	Memory VDD VID	MEM VID: pull-up to 3V3_AOH or pull-down to GND to set boot FBVDD/Q voltage
GPIO2	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO3	LCD_VCC	O	Panel Power Enable	LCD_VCC: 100k pull-down
GPIO4	LCD_BLEH	O	Panel Backlight Enable	100K pull-down
GPIO5	3V3_MAIN_EH	O	GPU power sequencing	10K pull-up to 3V3_AOH
GPIO6	FB_CLAMP_TGL_REQ	O	Clamp toggle request for GC6 1.0	10K pull-up to system 3.3V
	GPU_EVENT#	I	GPU wake signal for GC6 2.0	10K pull-up to 3V3_AOH
GPIO7	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO8	SYS_PEX_RST_MON#	I	System side PCIe reset Monitor	
GPIO9	ALERT	I/O	Active Low Thermal Alert	10K pull-up to 3V3_AOH
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	PWM_VID	O	GPU Core VDD PWM control signal	
GPIO12	PWR_LEVEL	I	AC power detect or powor supply overdraw input	100K pull-up to 3V3_AOH
GPIO13	PSI	O	Phase Shedding	10K pull-up to 3V3_AOH to enable two phase.
GPIO14	HPD_A	I	Hot Plug Detect for IFPA used as DisplayPort or for IFPAB when used as Dual Link DVI	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for IFPC	See Figure 12-1
GPIO16	RESERVED			
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	See Figure 12-1
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	See Figure 12-1
GPIO19	HPD_F or HPD_B	I	Hot Plug Detect for IFPF or for IFPB when used as DisplayPort	See Figure 12-1
GPIO20	Reserved			
GPIO21	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	10K pull-up to 3V3_AOH
OVERT	OVERT	O	Active Low Thermal Catastrophic Over Temperature	10K pull-up to 3V3_AOH



Project Name	X540UV/UA		Rev
Title :	N14M-GE_GPIO		
Dept.:		Engineer:	NB2_EE2
Date:	Thursday, September 01, 2016	Sheet	76 of 89

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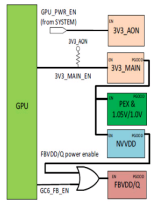
- 066_
- 067_***
- 068_B to B connector_HDD_ODD
- 069_EMI
- 070_VGA_nVIDIA_N16V/S_PCIE
- 071_VGA_nVIDIA_N16V/S_FB-IF
- 072_VGA_nVIDIA_N16V/S_FB-DDR3
- 073_VGA_nVIDIA_N16V/S_VDD
- 074_VGA_nVIDIA_N16V/S_DISPLAY
- 075_VGA_nVIDIA_N16V/S_ROM, XTAL
- 076_VGA_nVIDIA_N16V/S_GPIO
- 077_VGA_nVIDIA_N16V/S_POWER
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS



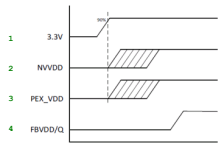
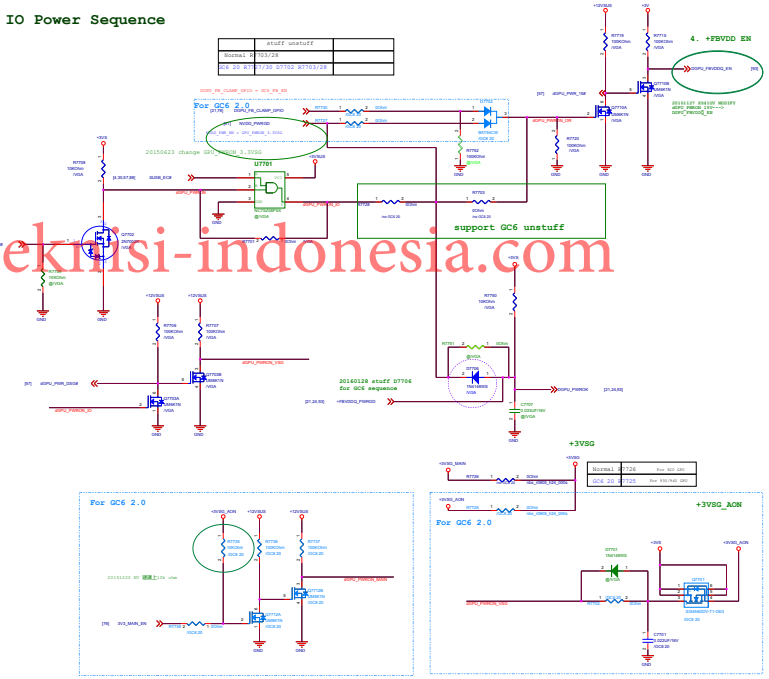
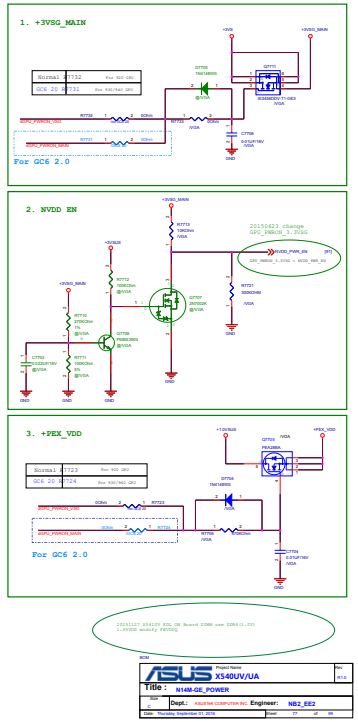


Figure 3-7. Example of Power-Up Sequencing Order

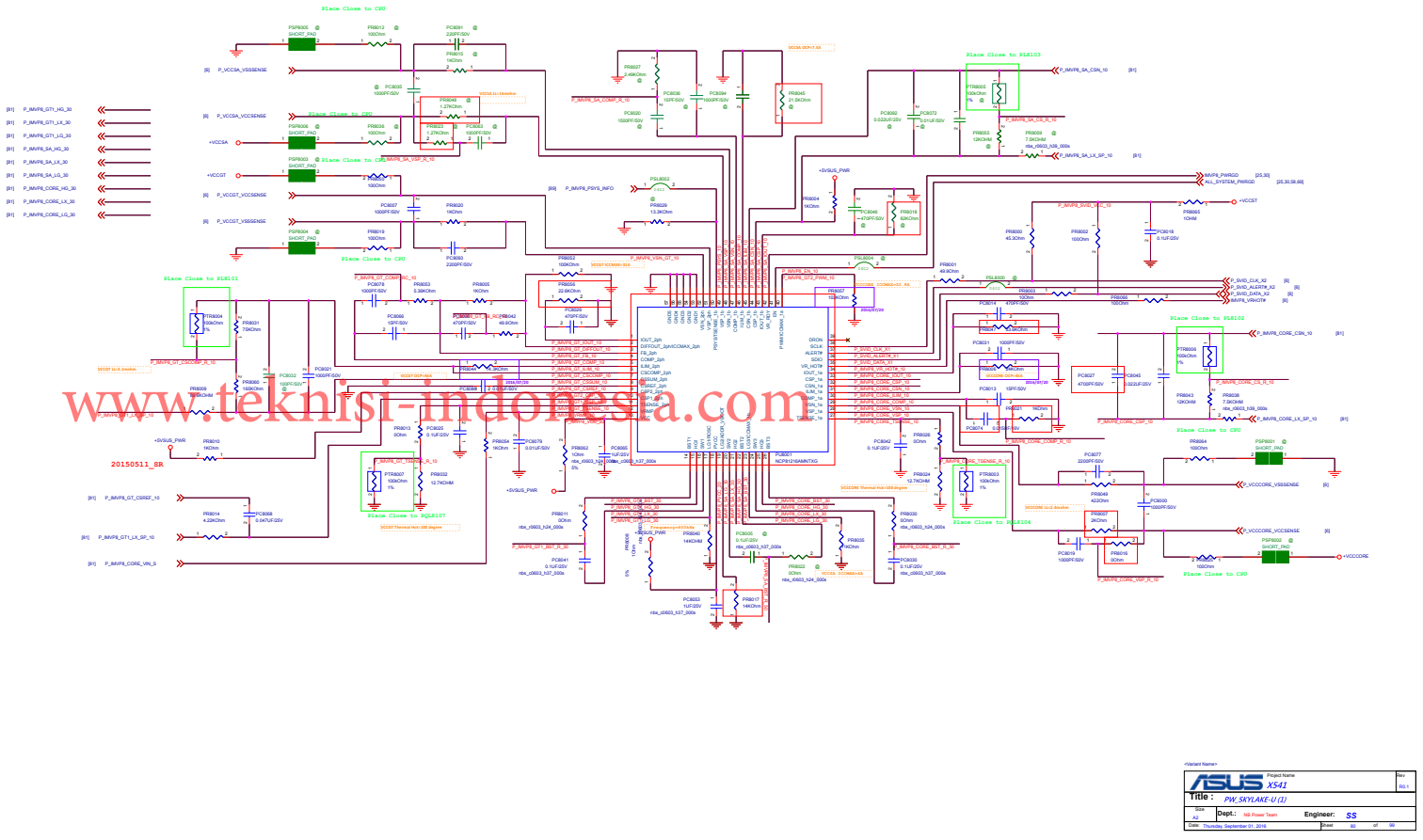
dGPU IO Power Sequence



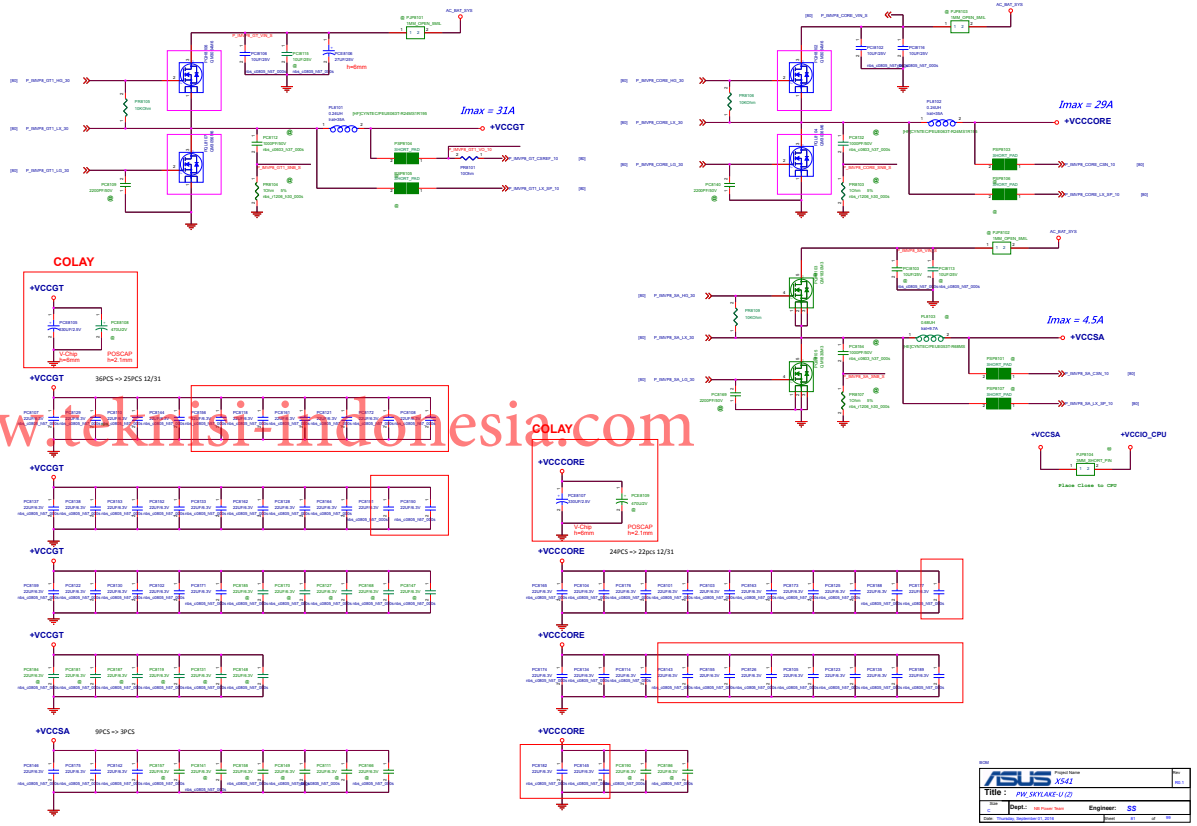
dGPU Core Power Sequence



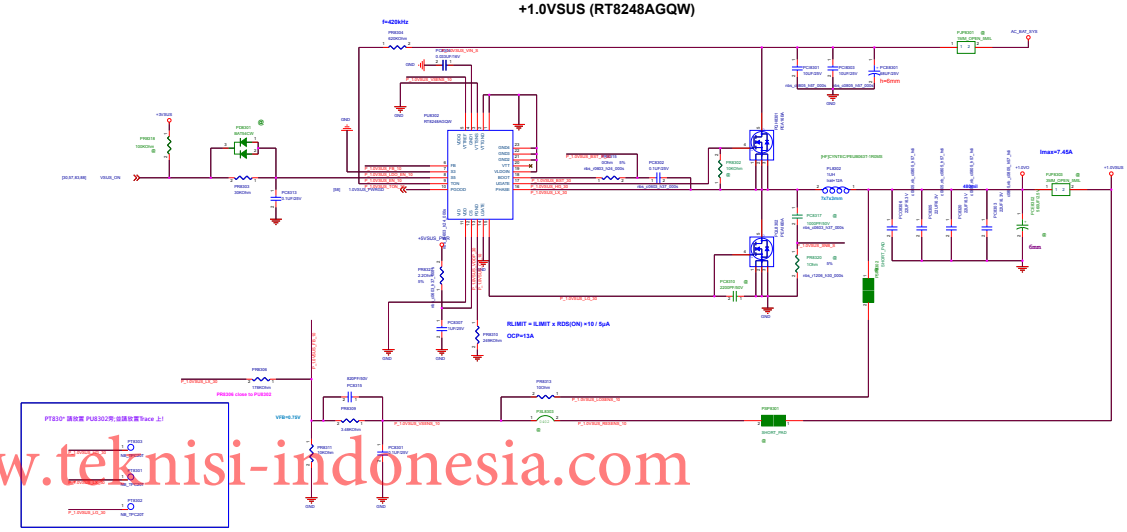
Skylake IMVP8 (1) Power [For CPU]



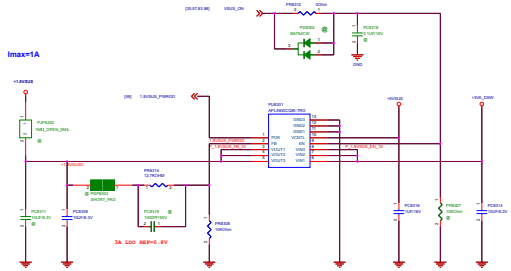
Skylake IMVP8 Power (2) [For CPU]



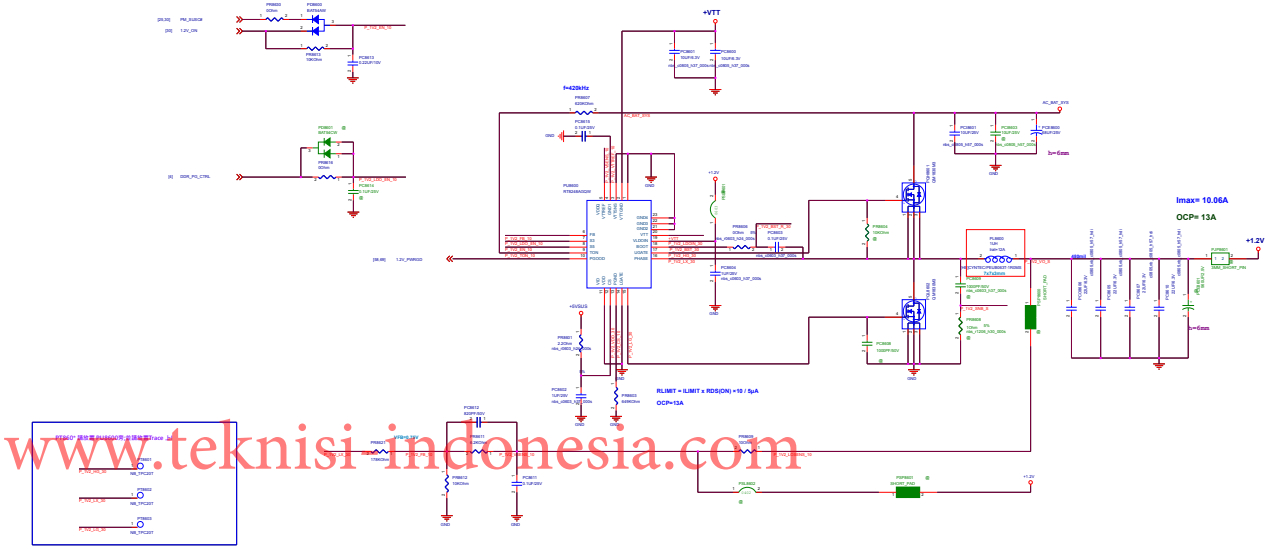
+1.0VSUS (RT8248AGQW)



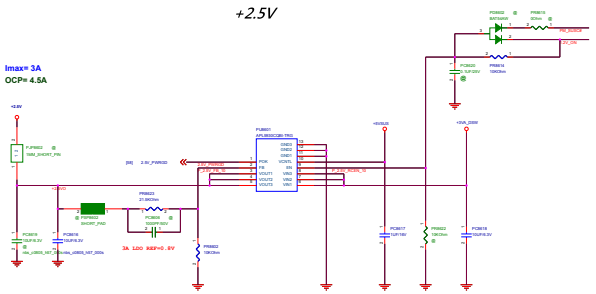
+1.8VSUS [For PCH]

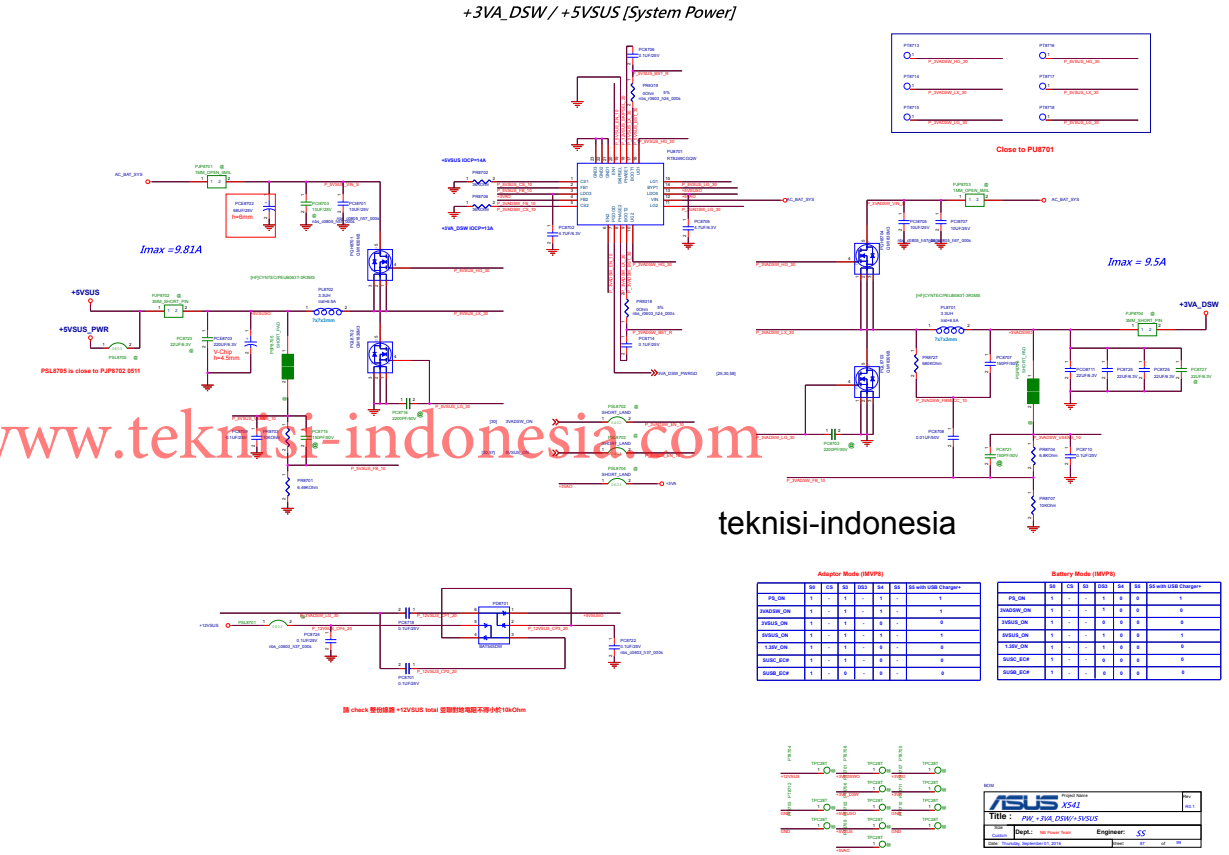


+1.2V / +VTT / +2.5V[For Memory]



+2.5V





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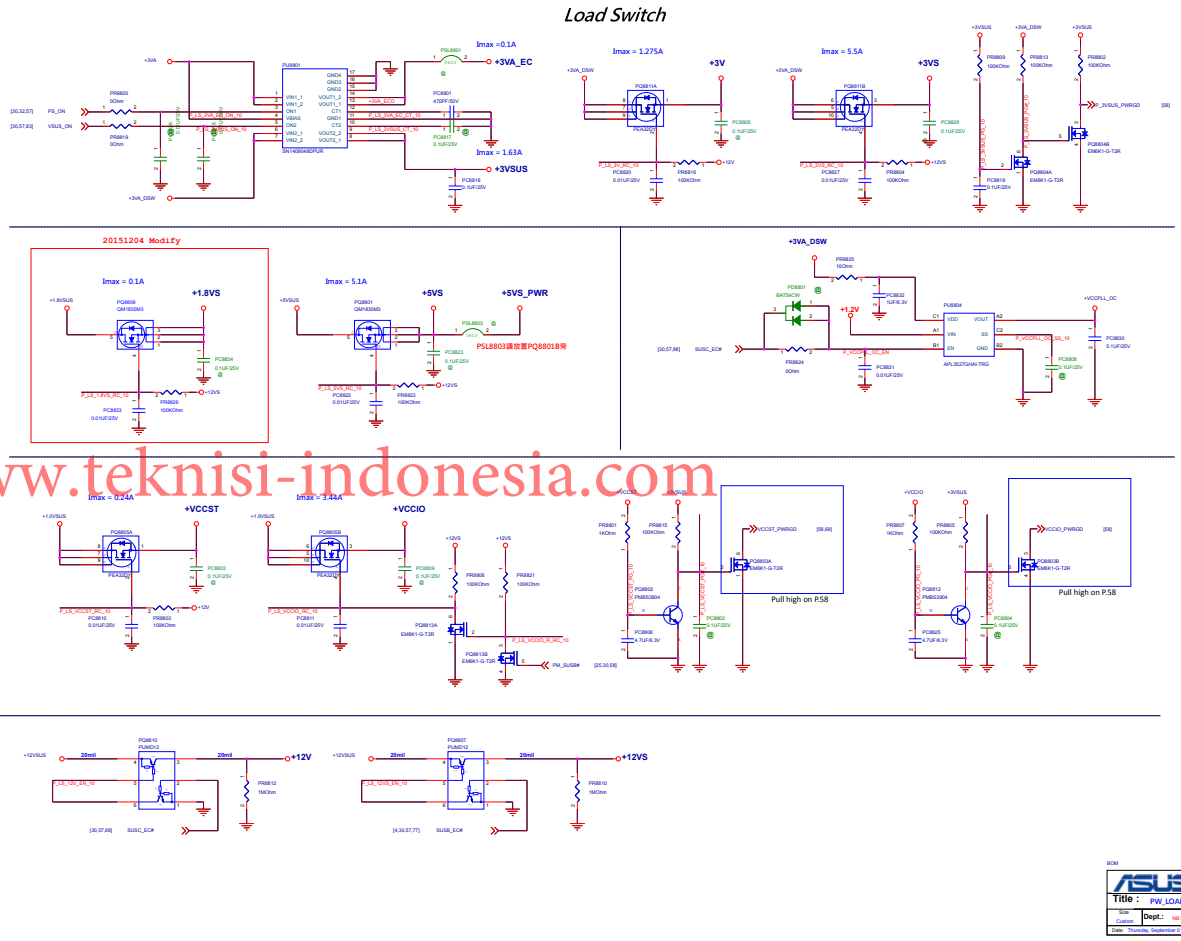
- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode



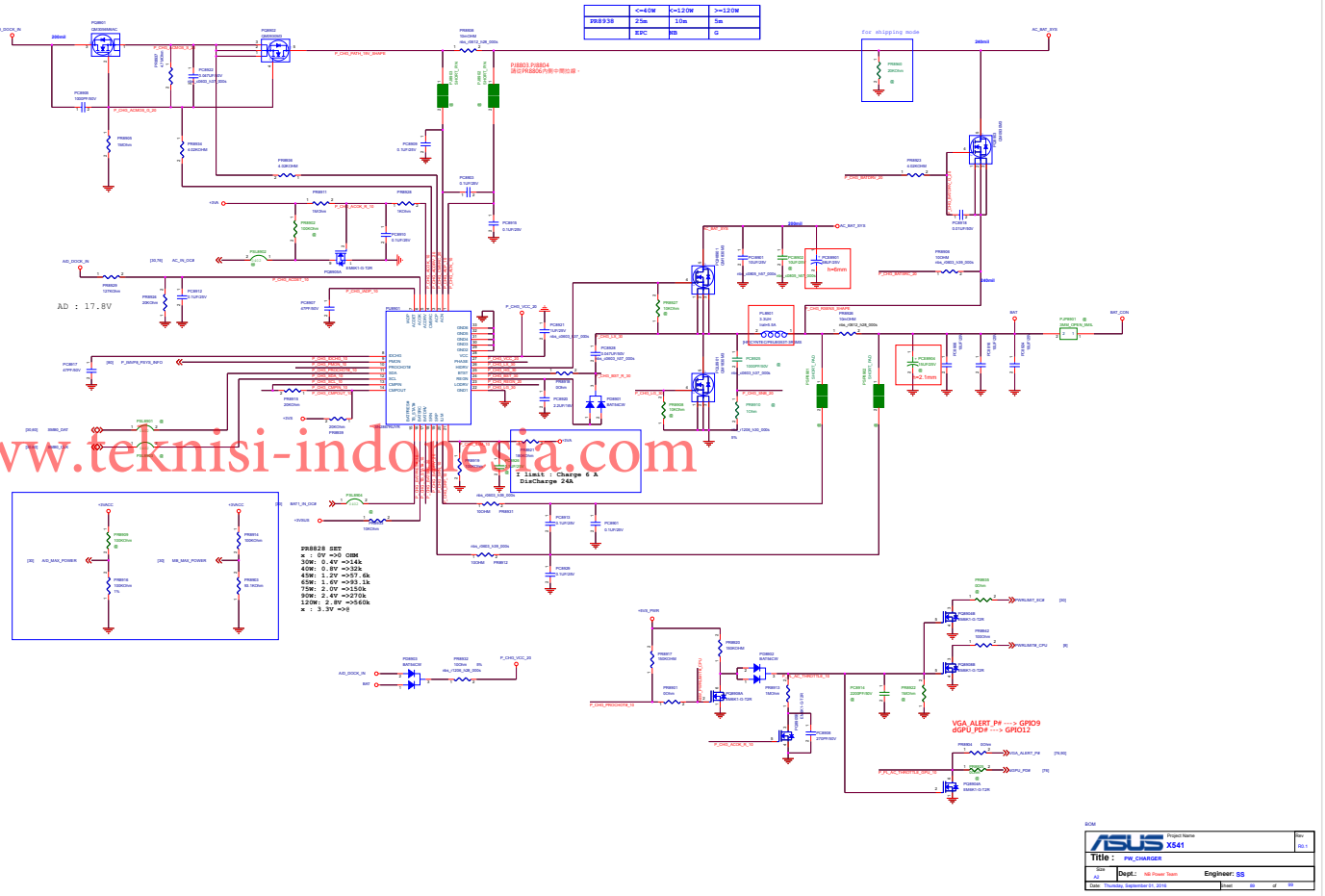
ASUS X541

Title : PW_LOAD_SWITCH

Dept.: NB Power Team Engineer: SS

Schematic Page List Hide

- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

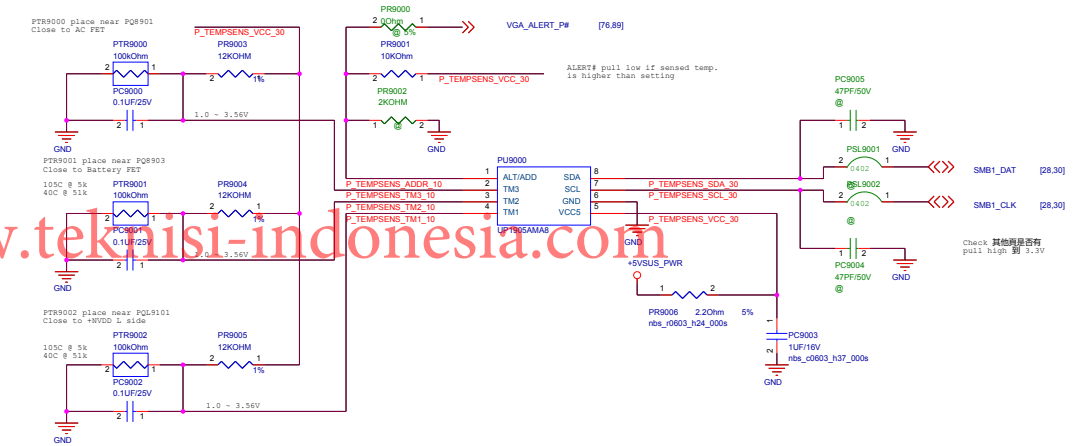


Address Selection Table

Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR9001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR9002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Register Address

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert



<Variant Name>

ASUS	Project Name: X541	Rev: R0.1
Title : PW_PROTECTION		
Size: A4	Dept.: NB Power Team	Engineer: SS
Date: Thursday, September 01, 2016	Sheet 90 of 102	

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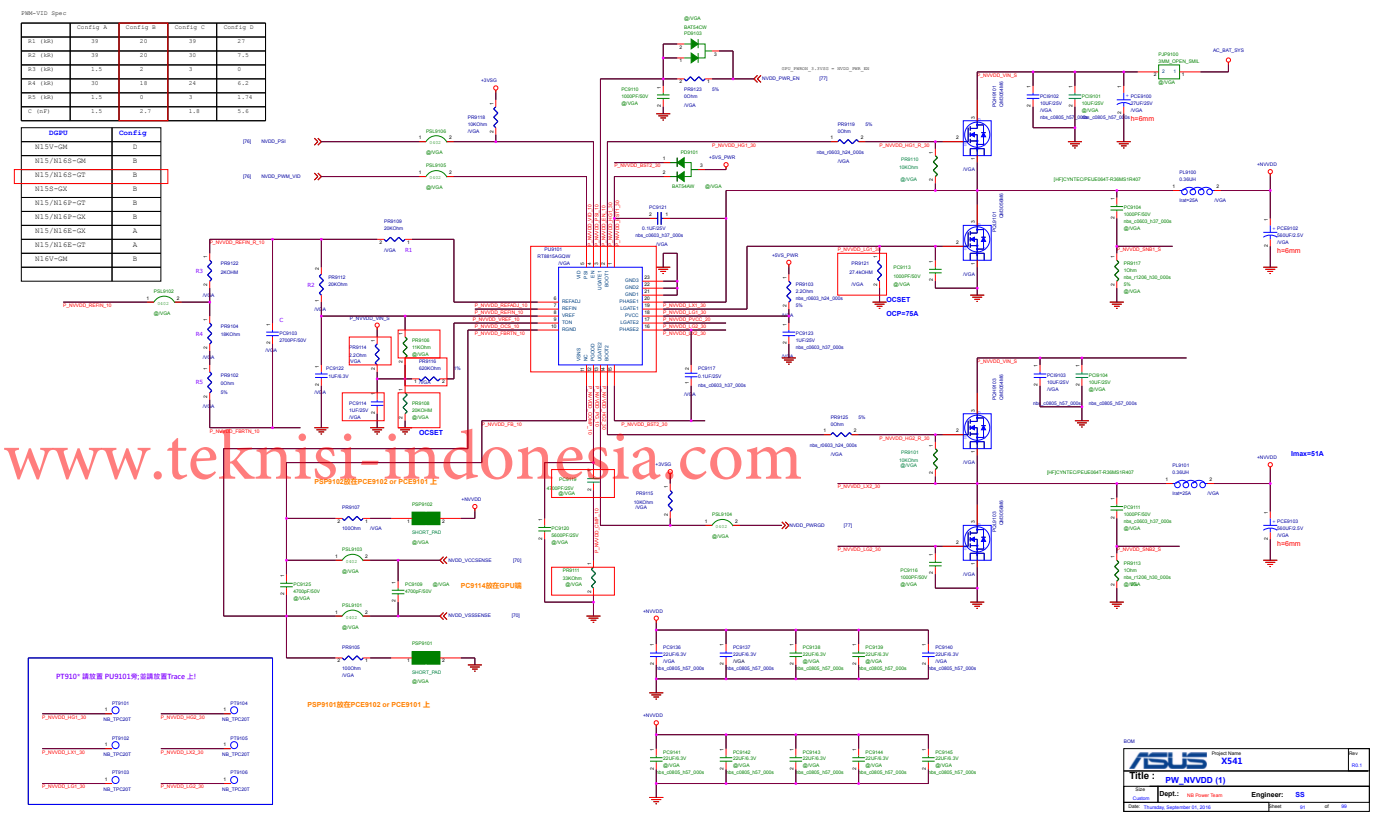
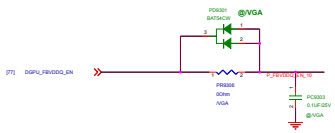
- R
- 078_VGA_****
- 079_VGA_****
- 080_PW_SKYLAKE-U (1)
- 081_PW_SKYLAKE-U (2)
- 082_PW_***
- 083_PW_+1.0VSUS/+1.8VSUS
- 084_PW_
- 085_PW_***
- 086_PW_+1.2V/+VTT/+2.5V
- 087_PW_+3VADSW/+5VSUS
- 088_PW_LOAD SWITCH
- 089_PW_CHARGER
- 090_PW_PROTECTION
- 091_PW_+NVVDD (1)
- 092_PW_***
- 093_PW_+FBVDDQ
- 094_PW_***
- 095_PW_***
- 096_PW_***
- 097_PW_
- 098_PW_***
- 099_PW_FLOW CHART
- 100_Power On Timing--AC mode
- 101_Power On Timing--DC mode

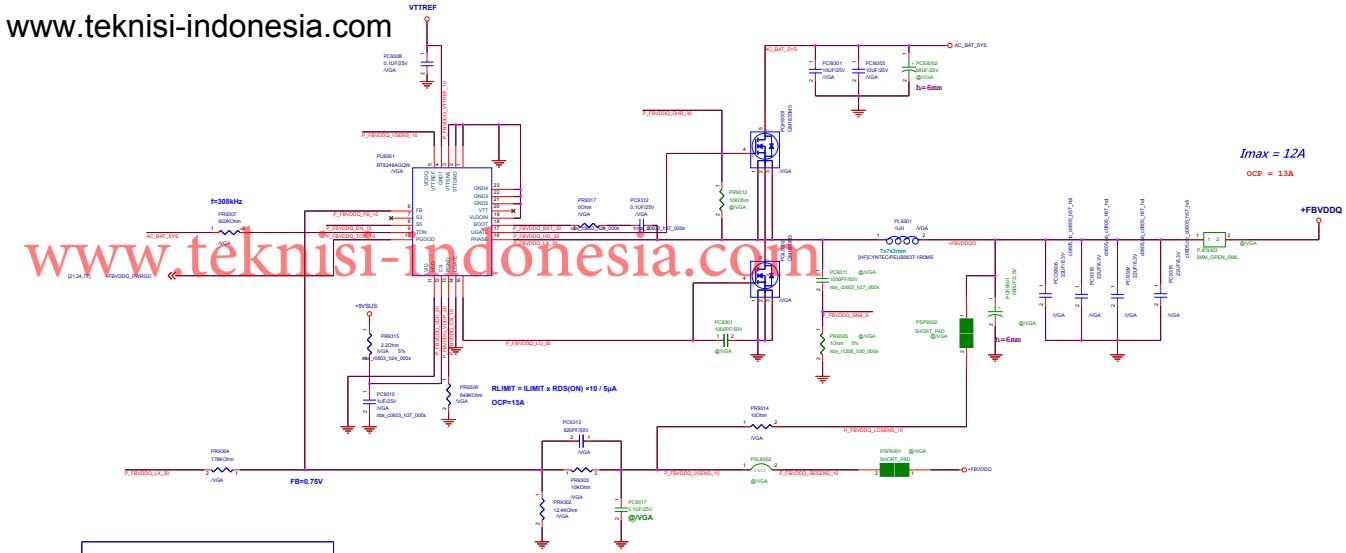


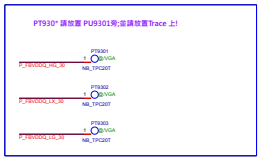
S3 And S5 Truth Table

State	Pin7(S3)	Pin8(S5)	VDDQ	VTTREF	VTT
S0	1	1	On	On	On
S3	0	1	On	On	OFF(Hi-Z)
S4/S5	0	0	OFF (Discharge)	OFF (Discharge)	OFF (Discharge)

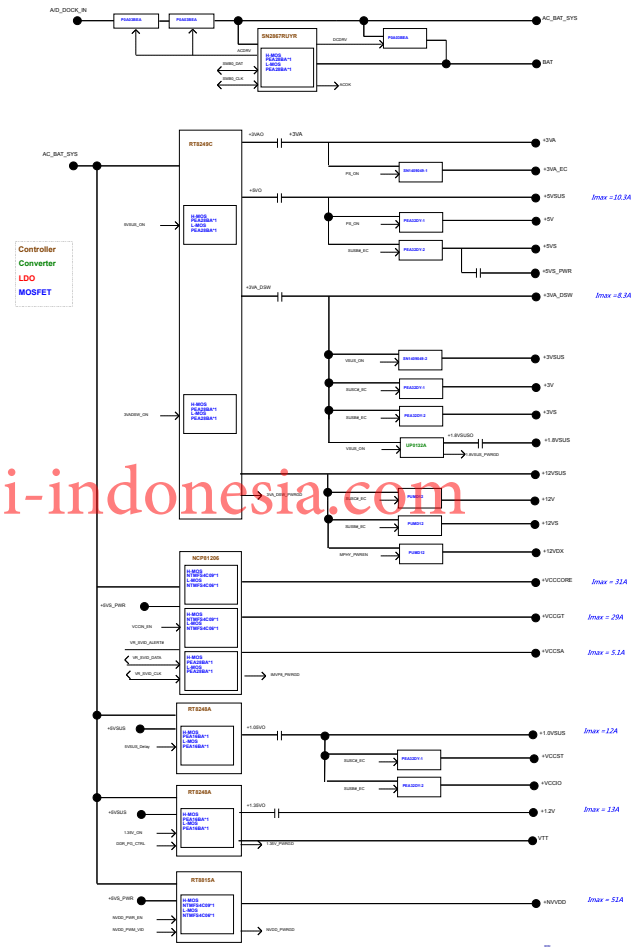


+FBVDDQ
[For FRAM]





Project Name	X541
Title :	PW_+FBVDDQ
Dept.:	NB Power Team
Engineer:	SS



ASUS X540UV/UA
Title : PWFLOWCHART
Engineer: POWER

ASUS X541UV/UA
Title : Power On Timing

ASUS X541UV/UA
Title : Power On Timing
Dept.: ASUSTeK COMPUTER INC. Engineer: